

A Novel Approach To Construct Online Testable Reversible Logic

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Abstract— Reversible logic is emerging as an important research area having its application in diverse fields. Reversible circuits can be used in the fields of low-power computation, cryptography, digital signal processing, communications and the emerging field of quantum computation. Regardless of the eventual technology adopted, testing is sure to be an important component in any robust implementation. A new approach for automatic conversion of any given reversible circuit into an online testable circuit that can detect online any single-bit errors, including soft error in logic block is described in this paper.

Keywords— Reversible logic; parity preserving reversible gates.

I. Introduction

Possibility of nearly energy-free computation is the primary motivation for the study of reversible circuits. Power dissipation is an important factor in VLSI design. Combinational logic circuits dissipate heat in an order of $kT \ln 2$ joules for every bit of information that is lost, where k is the Boltzman constant and T is the operating temperature [1]. Information is lost when the input vector can not be uniquely recovered from its output vectors. Reversible logic circuits naturally take care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors and therefore no information is lost. According to [2] zero energy dissipation would be possible only if the network consists of reversible gates. Thus reversibility will become an essential property in future circuit design. Synthesis of reversible logic circuits differs from the combinational one in many ways [3]. Firstly, in reversible circuit there should be no fan-out, that is, each output will be used only once. Secondly, for each input pattern there should be a unique output pattern. Finally, the resulting circuit must be acyclic. Any reversible gate performs the permutation of its input patterns only and realizes the functions that are reversible. If a reversible gate has k inputs, and therefore k outputs, then we call it a $k \times k$ reversible gate. Any reversible circuit design includes only the gates that are reversible. In a reversible circuit, the outputs that are not used as primary outputs are called garbages and the input lines that are set to constants are termed as constant inputs. An efficient design should keep the number of garbage outputs to minimum. Parity checking is one of the widely used error detection mechanisms in digital logic and data communication systems.

This is because most of the arithmetic functions is not parity preserving. If the parity of the input data is maintained throughout the computation, no intermediate checking would be required [4]. A sufficient requirement for parity preservation of a reversible circuit is that each gate be parity preserving [4]. In this paper I introduce a method by which we

can test parity preserving reversible circuit and not parity preserving reversible circuit.

II. Reversible Logic Circuit:

Reversible circuit is composed of reversible gates that there is a one-to-one relationship between its inputs and outputs. A gate is *reversible* if the Boolean function it computes is bijective. If a reversible gate has k input and output wires, it is called a $k \times k$ gate. A circuit is *reversible* if all gates are reversible and are interconnected without fan out or feedback. If a reversible circuit has n input and output wires, it is called an $n \times n$ circuit.

The fan-outs and feedback paths are not permitted in reversible logic.

Definition 1:

A reversible gate is a $k \times k$ gate, if it has k inputs and k outputs (Haghparsat, 2008).

Definition 2:

If the output is not used for future computations, the output is said garbage output (Haghparsat, 2008).

A. Basic Reversible Gates

There exist many reversible gates in the literature. Among them 2×2 Feynman gate (FG) [5], 3×3 Peres gate (PG) [6], 3×3 Toffoli gate (TG) [7], and 3×3 Fredkin gate (FRG) [8], have been studied extensively. Because of their simplicity and quantum realization cost there are design approaches and tools that incorporate them separately or in combination with each other.

B. Parity preserving reversible gate

The gate is a parity preserving reversible gate if and only if satisfy the follow equation. For example the equation for a reversible 3×3 gate is: $I_1 \oplus I_2 \oplus I_3 = O_1 \oplus O_2 \oplus O_3$

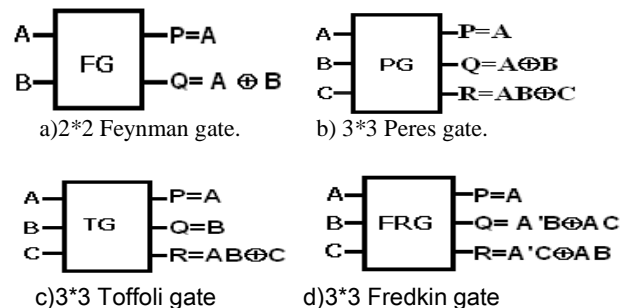


Fig 1. Some well-known reversible logic gates.

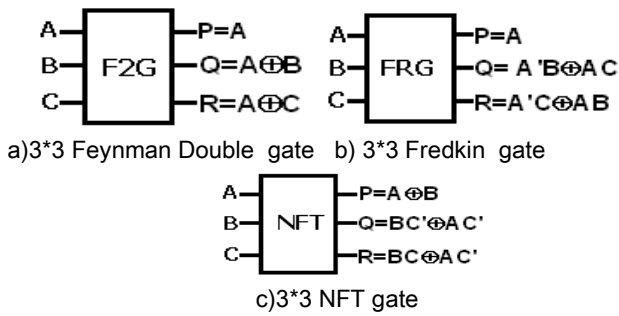


Fig 2. Some parity preserving reversible gates.

TABLE 1. TRUTH TABLE OF PARITY PRESERVING F2G GATE

I1	I2	I3	O1	O2	O3
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

TABLE 2 . TRUTH TABLE OF PARITY PRESERVING FREDKIN GATE

I1	I2	I3	O1	O23	O3
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

TABLE3. TRUTH TABLE OF PARITY PRESERVING NFT GATE

I1	I2	I3	O1	O2	O3
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	0	1

III. Proposed Testing Method

The proposed testing method will test a reversible circuit through a control line and detect any single bit error. This method is very simple to design so we need not invest much time to design a tester circuit with this method. And any type of reversible gate such as conservative gate, parity preserving gate or any other type of reversible gate can be tested with this method. After all of the line connected in a single line with XOR gate TC which is tester input signal will be calculated for that particular logic.

$$TC = I1 \oplus I2 \oplus \dots \oplus In \oplus O1 \oplus O2 \oplus \dots \oplus On$$

Now observe tester output signal (Z). If Z is equal to one then error detected.

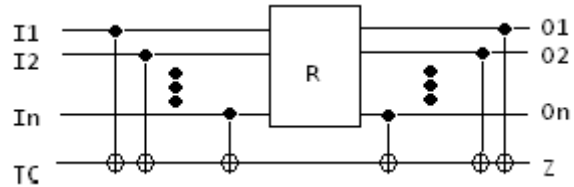


Fig 3. Online reversible gate testing through control line

For parity preserving reversible circuit only connect all input and output to a control line with XOR gate and initial value $TC = 0$. And expected output 1 for any single error. But at that stage we have to consider control line may be faulty so if there is fault to control line then it allows shows not faulty. If such doubt we check with initial value $TC = 1$ also; and expect 0 for arise any single error in circuit.

It will done because of parity preserving concept. So mathematically control output Z must be

$$TC \oplus A \oplus B \oplus C \oplus P \oplus Q \oplus R = 0$$

Where, $TC = 0$

For error free condition

Else error detect.

$$\text{And } TC \oplus A \oplus B \oplus C \oplus P \oplus Q \oplus R = 1$$

Where, $TC = 1$

For error free condition

Else error detect

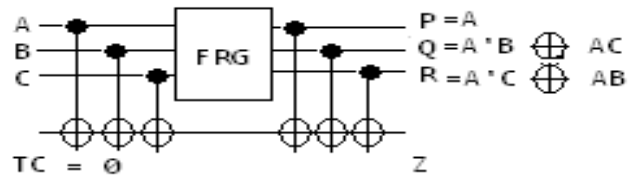


Fig 4. FRG parity preserving gate testing

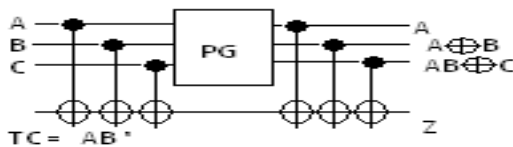


Fig 5. PERES gate testing

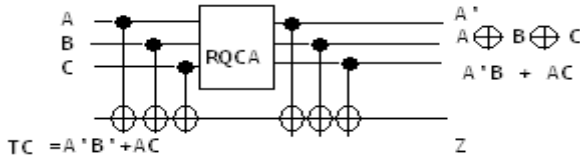


Fig 6 . RQCA gate testing

For not parity preserving reversible circuit we have not such fixed initial value. We fixed it (TC) by $f(A,B,C)$. Then after tester output (Z) will be observe correctly. This TC may be varied for deferent circuit. Here I have used Boolean logic for calculating TC or tester circuit function to convert into parity preserving. For example I have used 3*3 PERES gate to detect error in Fig 5. Calculating tester circuit for 3*3 PERES gate (not parity preserving reversible circuit) is bellow:

$$TC = A \oplus B \oplus C \oplus P \oplus Q \oplus R$$

It means by TC the circuit will be parity preserving. Then we can do same procedure for testing the circuit.

$$A \oplus B \oplus C \oplus P \oplus Q \oplus R \oplus TC = 0$$

[Where, TC = Tester Circuit or Initial value of control line]

$$\Rightarrow A \oplus B \oplus C \oplus A \oplus (A \oplus B) \oplus (AB \oplus C)$$

$$\oplus TC = 0$$

$$\Rightarrow (A'C + AC') \oplus (A'C + B'C + ABC') \oplus TC = 0$$

$$\Rightarrow (A'C' + AC) (A'C + B'C + ABC')$$

$$+ (AC' + ABC')(A' + B' + C) \oplus TC = 0$$

$$\Rightarrow AB'C + AB'C' \oplus TC = 0$$

$$\Rightarrow AB' \oplus TC = 0$$

$$\Rightarrow TC = AB'$$

TABLE4. TRUTH TABLE OF NOT PARITY PRESERVING REVERSIBLE PERES GATE

A	B	C	A	$A \oplus B$	$AB \oplus C$	TC
0	0	0	0	0	0	0
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	0	1	1	0
1	0	0	1	1	0	1
1	0	1	1	1	1	1
1	1	0	1	0	1	0
1	1	1	1	0	0	0

After fixing initial value TC with function we can join all the input and output in a single line by XOR operator. Then if there is any single error testing output will be high else low and for initial value TC' it will vise versa. And for any doubt about correctness of control line, pass initial value both TC and TC'.

It is clear that in parity preserving circuit we have not calculate this TC because it will always low for the circuit itself is parity preserving; no need of extra calculation.

Define Tester Signal in another circuit:

TABLE5. TRUTH TABLE OF NOT PARITY PRESERVING REVERSIBLE RQCA GATE

A	B	C	A'	$A \oplus B \oplus C$	$A'B + AB$	$TC = A'B' + AC$
0	0	0	1	0	0	1
0	0	1	1	1	0	1
0	1	0	1	1	1	0
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	1	0	0	1	1
1	1	0	0	0	0	0
1	1	1	0	1	1	1

So, TC initialize $A'B' + AC$ for RQCA gate[9] testing. And expect $Z = 1$ for any single bit error in RQCA gate Or expect $Z = 0$ for $TC = (A'B' + AC)'$ for single bit error in RQCA gate.

IV. Conclusion

This is very good method to construct online testable reversible circuit through a single testing line only by which we can detect any single bit error. Any type of reversible gate including parity gate, not parity gate and conservative logic gate can be testable through this approach. Not only that any large circuit which have no testable feature can be converted into a circuit with online testable feature with this method. We also considered the problem in which local communications as faulty control line. We can design tester circuit and connect with all input and output to test parity preserving reversible circuit and not parity preserving reversible circuit.


References

- [1] R. Landauer, "Irreversibility and heat generation in the computational process", IBM J. Res. Develop., vol. 5, pp. 183-191, 1961.
- [2] C. H. Bennet, "Logical reversibility of computation", IBM J. Res. Develop., vol. 17, no. 6, pp. 525-532, 1973.
- [3] M. S. Islam, and M. Rafiqul Islam, "Minimization of reversible adder circuits", Asian Journal of Information Technology, vol. 4, no. 12, pp. 1146-1151, 2005.
- [4] B. Parhami, "Fault tolerant reversible circuits", in Proceedings of 40th Asimolar Conf. Signals, Systems, and Computers, Pacific Grove, CA, pp. 1726-1729, October 2006
- [5] R. Feynman, "Quantum mechanical computers", Optical News, vol. 11, 1985, pp. 11-20.
- [6] A. Peres, "Reversible logic and quantum computers", Physical Review: A, vol. 32, no. 6, pp. 3266-3276, 1985.
- [7] T. Toffoli, "Reversible computing", In Automata, Languages and Programming, Springer-Verlag, pp. 632-644, 1980.



- [8] [E. Fredkin and T. Toffoli, "Conservative logic", Intl. Journal of Theoretical Physics, pp. 219-253, 1982.
- [9] Bibhash Sen, Manojit Dutta, Debajyoty Banik, Dipak K Singh and Biplab K Sikdar," Design of Fault Tolerant Reversible Arithmetic Logic Unit in QCA", ISED, 2012

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