

# Design of Sequential circuits using Threshold Logic

Mili Sarkar, Prasenjit Sengupta, Shilpi Raj

**Abstract**— *In this paper we propose an implementation technique for sequential circuit using threshold logic. With the advancement of nano technology threshold gate based logic design has got a new direction. In this paper first negative edge triggered D flip-flop has been designed. Then negative edge triggered T flip-flop has been designed. Finally threshold gate based counter has been realized. The proposed design has been verified by means of simulation using VHDL.*

**Keywords**—*Threshold logic gates, Single electron tunneling (SET), Resonant tunneling diode (RTD), Counter, Very Large Scale Integration (VLSI).*

## I. Introduction

The impact of VLSI technology has made nano system design a very lively research topic. Even more nano electronics devices such as SET or RTDs can be used for threshold logic implementation. Besides, there are many theoretical results showing that TL circuits are more powerful than classical Boolean circuits. A logical function which is linearly separable[6] can be designed using threshold logic[3]. The design style of latches and flip-flops using single electron tunneling technology based threshold logic already reported. In this process charge is transported through SET transistor[4]. Earlier investigations have revealed that SET logic gates operate according to the single electron encoded logic paradigm[7].

Design of sequential circuits using single electron encoded logic is also reported in[5]. The remainder of this paper is organized as follows-

Section-II introduces the SET theory explaining the charge transport behaviour appearing in SET circuits and the SET buffer which are combined as a generic SEEL buffer threshold logic[8].

Section-III introduces the Threshold Logic Gates can be also designed using resonant tunneling diodes (RTD)[9]. RTD has promising features due to its high speed switching capability and functional versatility.

Section-IV investigates the threshold gate based negative edge triggered D-flip-flop, T-flip-flop and their output waveforms.

## II. Background of SET and Generic Threshold Gate

It is widely known that the ever decreasing feature size and the corresponding increase in the number of transistors per millimeters squared facilitated vast improvements in semiconductor based designs. It is also understood that such improvement will eventually come to an end.

Single electron devices work on the principle of Coulomb Blockade to transfer a single electron charge and provide an alternative way to realize digital logic [1]. The SET devices have got the advantages of fast and low power operation because they use only one electron to do logic and arithmetic operations [16].

Single electron logic is to encode Boolean values directly as single electron charges. One approach in this direction is based on the physical transport of the charge from one gate to another, such that Boolean input signals consist of the presence of absence of the arriving charge. When charge transport is scaled down to just one electron, this approach leads to single electron encoded logic (SEEL) logic gates and memory elements, in which the Boolean logic values 0 and 1 are encoded as a net charge of zero and one electron charge only[12].

A tunnel junction can be thought of as a leaky capacitor. The transport of charge through a tunnel junction is referred to as tunneling, where the transport of a single electron through a tunnel junction is referred to as a tunnel event.

We assume that all conditions are met such that charge quantization is observable ( $E_c \gg E_q$ ) and that tunnel events due to thermal energy can be ignored ( $E_c \gg k_B T$ ). Under these conditions, the critical voltage  $V_c$  across a tunnel junction is the voltage threshold that is needed across the tunnel junction in order to make a tunnel event through this tunnel junction possible.

For calculating the critical voltage of a junction, we assume a tunnel junction with a capacitance of  $C_j$ . The remainder of the circuit, as viewed from the tunnel junction's perspective, has an equivalent capacitance of  $C_e$ . We calculate the critical voltage  $V_c$  for the junction as-

$$V_c = e / 2(C_e + C_j)$$

We refer to the charge of the electron as  $q_e = 1.602 \times 10^{-19} \text{ C}$ .

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### A. Threshold logic gates

Threshold Logic Gates are devices that are able to compute any linearly separable Boolean function given by-

$$Y = \text{sgn} \{F(x)\} = \begin{cases} 0, & \text{if } F(x) < 0 \\ 1, & \text{if } F(x) \geq 0 \end{cases} \quad (1)$$

$$F(x) = \sum_{i=1}^n w_i x_i - \psi \quad (2)$$

Where  $x_i$  is the  $n$  Boolean inputs and  $\omega_i$  is the corresponding  $n$  integer weights. The LTG compares the weighted sum of inputs and the threshold value  $\psi$ . If the weighted sum of inputs is greater than or equal to the threshold, the gate produces a logic 1. Otherwise, the output is logic 0.

Figure 1(a) depicts a generic SEEL threshold gate already been proposed earlier in (2). The threshold gate can be implemented using both positive and negative weights. Figure 1(b) displays a non-inverting static buffer. It can also be modified to form an inverting static buffer [11].

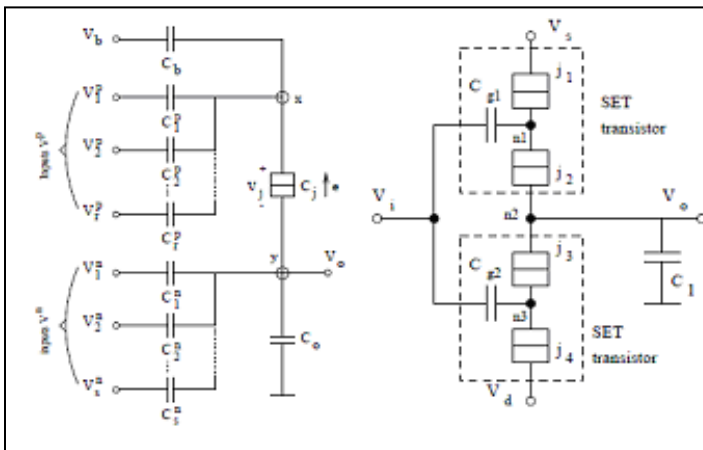


Figure. 1 (a) n-input LTG (b) Non-Inverting Buffer

The SET threshold gate combined with either inverting or non-inverting static buffer forms the basic building block for any threshold gate network. In our investigation we have used this basic building block to design various Boolean logic functions that forms the fundamental blocks for any digital circuit. The basic Boolean function AND, OR, NAND, NOR and NOT can be represented in the form of (1) and (2) as follows-

- AND(a,b) =  $\text{sgn}\{a+b-2\}$
- OR(a,b) =  $\text{sgn}\{a+b-1\}$
- NAND(a,b) =  $\text{sgn}\{-a-b+1\}$
- NOR(a,b) =  $\text{sgn}\{-a-b+0.5\}$
- NOT (a) =  $\text{sgn}\{-a+0.5\}$

### III. RTD analysis

TLGs are simulated using circuit models of RTD and FET in SPICE. The models are derived from piecewise linear isolation of the I-V characteristics of these devices. The principle of operation of the proposed logic gates is based on monostable bistable latch enable(MOBILE), which is a well

documented technique employing the latching capability of RTD. Two input AND gate and majority gate are designed and tested. The circuit demonstrates how small-scale threshold logic gates implementing standard Logic functions can be used to replace conventional Boolean gates and achieve reduced circuit complexity.

### A. Resonant Tunneling Diode

The RTD schematic symbol and its I-V curve are shown in Figure 2(a) and 2(b) respectively. RTD devices feature a nonlinear I-V characteristic that exhibits a region of negative differential resistance (NDR). When current  $I_{RTD}$  is smaller than its peak value  $I_P$ , it increases as  $V_{RTD}$  increases. The RTD is at a low resistance state.

Once  $I_{RTD}$  reaches  $I_P$ , the RTD enters the NDR region and  $I_{RTD}$  decreases as  $V_{RTD}$  increases.

The RTD switches to a high resistance state. Many important circuit functionalities can be enabled by exploiting this special NDR characteristic. [11]

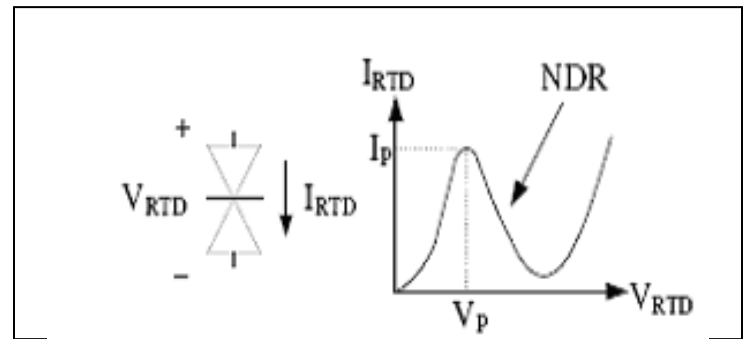


Figure. 2 (a) RTD schematic symbol (b) I-V Characteristics

The elementary unit of RTD based threshold logic gate (TLG) is the Monostable Bistable Logic Element (MOBILE). It consists of two RTDs driven by a  $V_{bias}$  as shown in fig.3. Circuit applications of RTDs are mainly based on the MOBILE. When  $V_{bias}$  is low both RTDs are in ON state.

With increasing  $V_{bias}$ , device with lowest peak current switches from ON state to OFF state. Output is HIGH if driver switches. Output is LOW if load switches. Peak currents are proportional to RTD Areas  $\lambda_1$  &  $\lambda_2$ .

If  $\lambda_1 < \lambda_2$   $V_{out} = 0$

If  $\lambda_2 < \lambda_1$   $V_{out} = 1$  Logic functionality can be achieved if the peak current of one of the RTDs is controlled by an input.

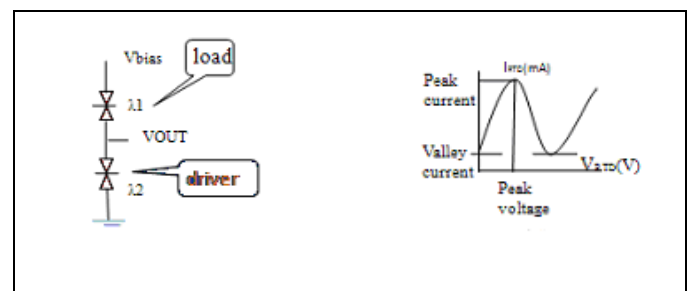


Fig.3 (a) Basic MOBILE structure, (b) I-V characteristics of RTD

## A. Design of Threshold Logic Gates

Table 3- Binary representation of AND function

X1	X2	F
0	0	0
0	1	0
1	0	0
1	1	1

INPUTS: {X1, X2}

CONDITIONS:

Both inputs are zero:

$$I_d - I_t < 0$$

$$(W_1X_1 + W_2X_2) A I_{pd} - T A I_{pd} < 0$$

$$(W_1X_1 + W_2X_2) - T < 0$$

$$(W_1X_1 + W_2X_2) < T$$

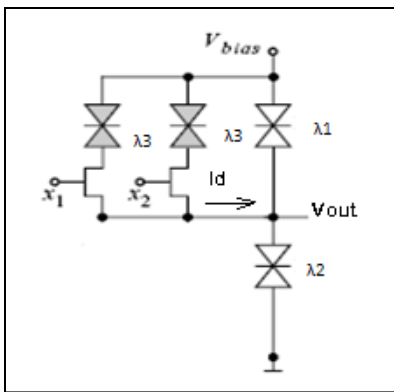


Fig.4 AND function implementation

Putting  $T = \lambda_2 - \lambda_1$ ,  $W_1 = \lambda_3$ ,  $W_2 = \lambda_3$ ,  
 $X_1 = X_2 = 0$

$$\lambda_1 < \lambda_2$$

(ii) One input is one:

$$I_d - I_t < 0$$

$$(W_1X_1 + W_2X_2) A I_{pd} - T A I_{pd} < 0$$

$$(W_1X_1 + W_2X_2) - T < 0$$

$$(W_1X_1 + W_2X_2) < T$$

Putting  $T = \lambda_2 - \lambda_1$ ,  $W_1 = \lambda_3$ ,  $W_2 = \lambda_3$

$X_1 = 0, X_2 = 1$  or  $X_1 = 1, X_2 = 0$

$$\lambda_3 < \lambda_2 - \lambda_1$$

$$\lambda_2 > \lambda_1 + \lambda_3$$

(iii) Both inputs are one

$$I_d - I_t > 0$$

$$(W_1X_1 + W_2X_2) A I_{pd} - T A I_{pd} > 0$$

$$(W_1X_1 + W_2X_2) - T > 0$$

$$(W_1X_1 + W_2X_2) > T$$

Putting  $T = \lambda_2 - \lambda_1$ ,  $W_1 = \lambda_3$ ,  $w_2 = \lambda_3$ ,  $X_1 = X_2 = 1$

$$2\lambda_3 > \lambda_2 - \lambda_1$$

$$\lambda_2 < \lambda_1 + 2\lambda_3$$

Hence, the conditions for AND function realization are

$$\lambda_1 < \lambda_2$$

$$\lambda_2 > \lambda_1 + \lambda_3$$

$$\lambda_2 < \lambda_1 + 2\lambda_3$$

The above conditions can be satisfied by taking  
 $W_1 = W_2 = 2$ ,  $T = 3$  ( $\lambda_2 = 4$ ,  $\lambda_1 = 1$ )

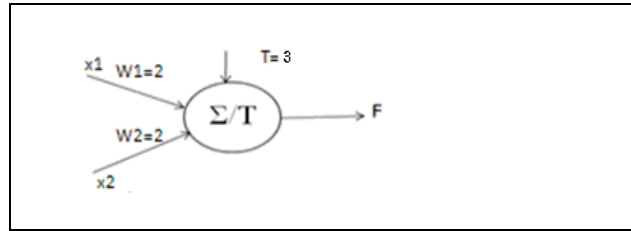


Fig. 5 Implementation of threshold logic AND Gate

## iv. Boolean Gate Based Memory Elements and Implementation with Threshold Logic.

Here, we investigate Boolean gate based implementations of D-Flip-flop, T-Flip-flop.

### A. Edge Triggered D-Flip-flop implementation

An edge triggered D-Flip-flop is easily implemented by adding a single inverter to the edge triggered JK flip-flop as shown in the figure 6.

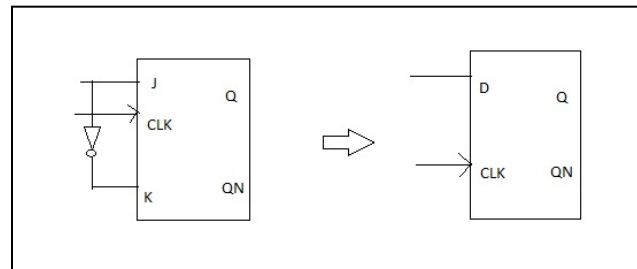


Fig. 6 “D-Flip-flop using JK-flip-flop”

Thus we can see that an edge triggered D-Flip-flop is a memory element with two inputs (D and clock) and two outputs (Q and its complement QN). We can summarize the behaviour of the negative edge triggered D flip-flop as follows-

Functional Truth Table of the Negative Edge Triggered D flip-flop:

Clock	D	Q	QN
1→0	0	0	1
1→0	1	1	0
0	0	Last Q	Last QN
0	1	Last Q	Last QN
1	0	Last Q	Last QN
1	1	Last Q	Last QN

### B. Threshold Gate Based negative edge triggered D-Flip-flop

It is known that any Boolean logic function can also be realised by a network of threshold logic gates (section II) [13]. A common implementation of a negative edge triggered D – flip-flop is a cascade of two D-latches in which the output Q of the first D-latch behaves as the input D of the second latch and the clock is connected directly to the input L of the first latch, while the input L of the second clock is connected to NOT (clock).

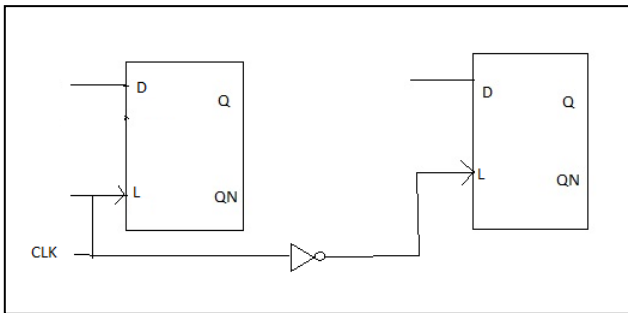


Fig.7 “Negative edge triggered D-flip-flop”

The resulting threshold gate based equations are:

$$A = \text{tlg1} = \text{sgn}(L - D + 1);$$

$$B = \text{tlg2} = \text{sgn}(2A - L - Q - 1);$$

$$C = \text{tlg3} = \text{sgn}(B - L + 1);$$

$$D = \text{tlg4} = \text{sgn}(2C - Q + L - 2);$$

The resulting threshold logic gate based negative edge triggered D-Flip-flop implementation is proposed, as shown in the figure 8:

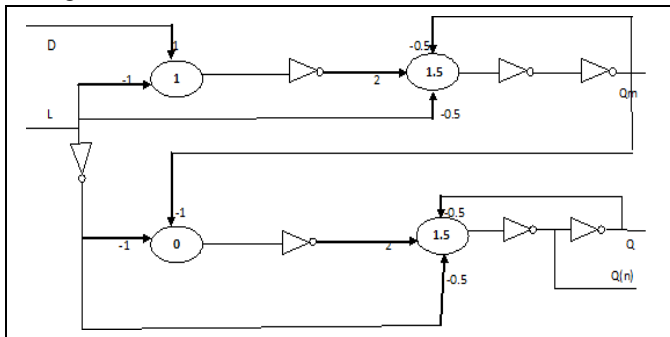


Fig.8 “D-Flip-flop using Threshold logic”

We have verified the proposed D-flip-flop implementation by using the VHDL simulator. The simulation results thus obtained are shown below in figure 9.

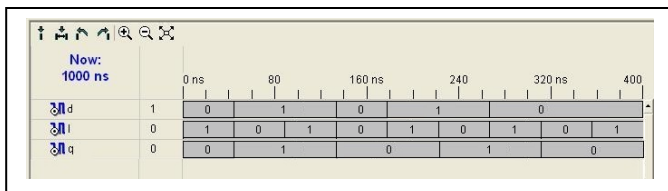


Fig.9 “D-Flip-flop waveform”

### C. Negative Edge Triggered T-flip-flop Implementation:

The designation ‘T’ comes from the ability of the flip-flop to “toggle”, or change state. Regardless of the present state of the flip-flop, it assumes the compliment state when the falling edge clock pulse occur when input ‘T’ is logic ‘1’. A negative edge Triggered ‘T’ flip-flop is cascade of two T- latches as shown :

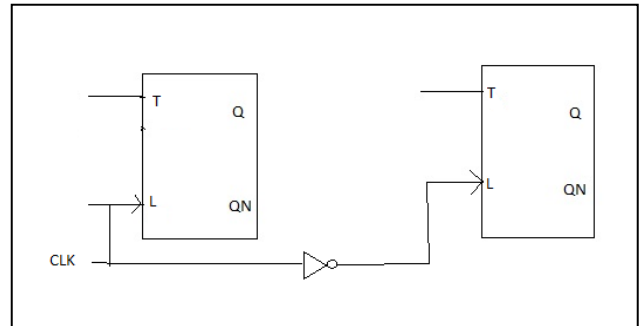


Fig.10 “T-latch based negative edge triggered T-flip-flop”

Now, the resulting behaviour of T-flip-flop can be summarized in table-

Functional Truth Table of the Negative Edge Triggered T flip-flop:

Clock	T	Q	QN
1→0	0	Last Q	Last QN
1→0	1	Complement Last Q	Complement Last QN
0	0	Last Q	Last QN
0	1	Last Q	Last QN
1	0	Last Q	Last QN
1	1	Last Q	Last QN

The resulting threshold logic gate based negative edge triggered T-flip-flop implementation is proposed, as shown in the figure.

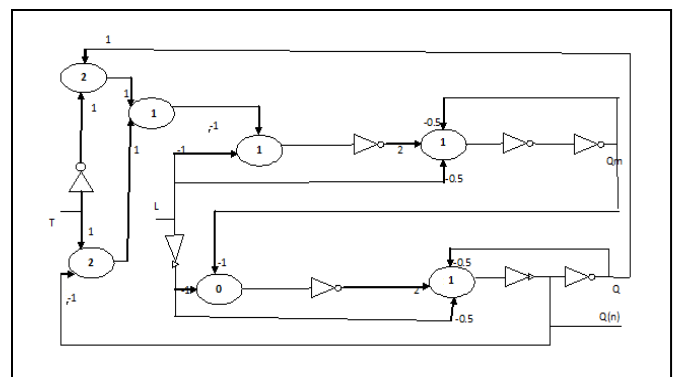


Fig.11 “Negative Edge Triggered T-flip-flop using threshold logic”

The threshold gate based equations which are used to make above circuit are written below:

$$\begin{aligned} A &= \text{tlg1} = \text{sgn}(T-Q-1); \\ B &= \text{tlg2} = \text{sgn}(Q-T-1); \\ C &= \text{tlg3} = \text{sgn}(A+B-1); \\ D &= \text{tlg4} = \text{sgn}(L-C+1); \\ E &= \text{tlg5} = \text{sgn}(2D-L-Q-1); \\ F &= \text{tlg6} = \text{sgn}(E-L+1); \\ G &= \text{tlg7} = \text{sgn}(2F-Q+L-2); \end{aligned}$$

We have verified the negative edge triggered T-flip-flop implementation by using the VHDL simulator. The simulation results thus obtained are shown below in figure 12:

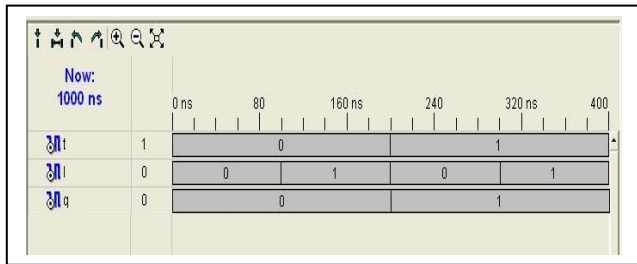


Fig.12 “T-flip-flop waveform”

## v. Design of two bit asynchronous counter using T-flip-flop:

In this type of counter, where each T-flip-flop output serves as the clock input signal for the next flip-flop, is referred to as an “asynchronous counter”. This is because all the flip-flops do not change status in exact synchronism with the clock pulses; only flip-flop A responds to the clock pulses flip-flop B has to wait for flip-flop A to change states before it is toggled.

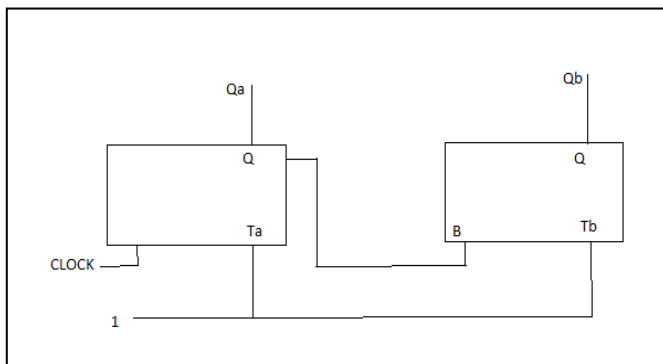


Fig.13 “Two bit asynchronous counter using T-flip-flop”

Now the resulting behaviour of this asynchronous counter is in table shown below:

Clock	Ta	Tb	Qa(LSB)	Qb(MSB)
1	1	1	0	0
0	1	1	1	0
1	1	1	1	0
0	1	1	0	1
1	1	1	0	1
0	1	1	1	1
1	1	1	1	1
0	1	1	0	0

The threshold gate based equations which are used to make above circuit are written below:

$$\begin{aligned} A &= \text{tlg1} = \text{sgn}(T-Q-1); \\ B &= \text{tlg2} = \text{sgn}(Q-T-1); \\ C &= \text{tlg3} = \text{sgn}(A+B-1); \\ D &= \text{tlg4} = \text{sgn}(L-C+1); \\ E &= \text{tlg5} = \text{sgn}(2D-L-Q-1); \\ F &= \text{tlg6} = \text{sgn}(E-L+1); \\ G &= \text{tlg7} = \text{sgn}(2F-Q+L-2); \\ H &= \text{tlg8} = \text{sgn}(Q-H-1); \\ I &= \text{tlg9} = \text{sgn}(1-q4-H); \\ J &= \text{tlg10} = \text{sgn}(2I-H-q4-2); \end{aligned}$$

The threshold gate based negative edge triggered two bit asynchronous counter is implemented as shown in figure.13

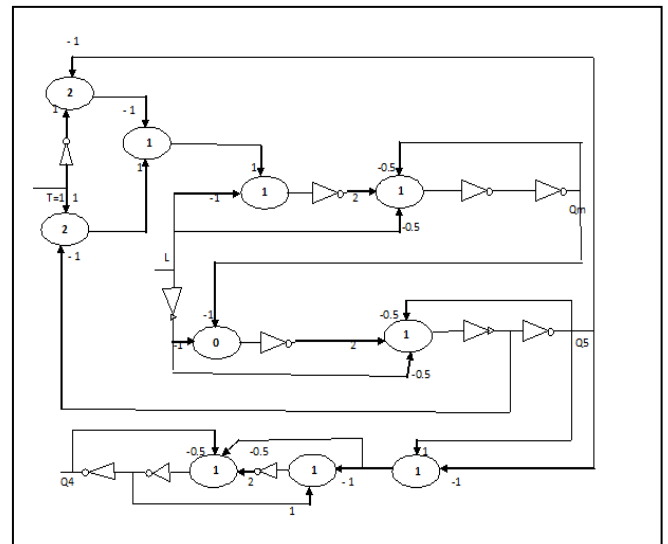


Fig.13 “Two bit asynchronous counter using threshold logic”

We have verified the two bit asynchronous counter implementation by using the VHDL simulator. The simulation results obtained is shown in figure14:

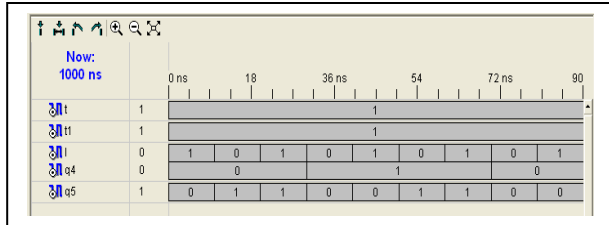


Fig.14 “Two bit asynchronous counter waveform”

## vi. Conclusion:

In this work, we proposed threshold gate based implementations of the D-flip-flop, T-flip-flop and asynchronous counter. The threshold gate based design of asynchronous counter needs less number of threshold logic gates which reduces the delay. We know that asynchronous counter is a sequential combination of T-flip-flops. To design a T-flip-flop through threshold logic we need seven threshold logic gates. But we observe that a two bit asynchronous counter can be designed by ten threshold logic gates. That means four threshold logic gates have been reduced which also reduces power consumption and delay.

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