A Review of Interleavers for IDMA systems

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Abstract—**Interleavers play a key role in interleave division multiple access (IDMA). In IDMA the separation of the information of different users is achieved by interleaving. Criteria for a good interleaver design for IDMA include low memory requirement, easy generation, low complexity, low correlation among interleavers, low overhead for synchronization between user and base station. In this paper we are giving a review of different interleavers.**

Key words **- random interleaver (RI), power interleaver (POI), tree based interleaver (TBI), shifting interleaver (SI), 2-dimension interleaver (2-DI), parallel interleaver (PI), prime number based interleaver (PNBI), linear congruential interleaver (LCI).**

I. INTRODUCTION

Multiple access schemes are an important means of providing communicational needs in a multi-user environment. Among these, code division multiple access (CDMA) system has been successfully deployed in many countries. In multiple access schemes, as a means of improving performance, forward error correction coding (FEC) has been utilized. For a coded CDMA system in multi-user transmission environments, iterative decoding and soft interference cancellation based on MMSE filter as part of multi-user detection (MUD) and decoding has been studied [1].

A new multiple access scheme called interleave-division multiple access (IDMA) was recently proposed [2], [3]. The IDMA combined with MISO has also been proposed, using partial CSI at the transmitters. This system employs iterative receiver structure to achieve partial cancellation of the cross antenna interference [4]. An interesting comparative analysis between CDMA and IDMA in iterative multi-user detections has been made and showed the superiority of IDMA over CDMA [5].

Interleaver is the only means to separate users in IDMA system [1]-[5]. In order to immunize noise and Multiple Access Interference (MAI) at the receivers, choosing interleavers which are weakly correlated between different users is very important.

In this paper we are comparing the performance of different type of interleavers. This paper is organized as follows. IDMA system model is given in section II. Different interleaving techniques are summarized in section III. Performance analysis is provided on section IV. Finally some conclusion of this paper and future work is given on section V.
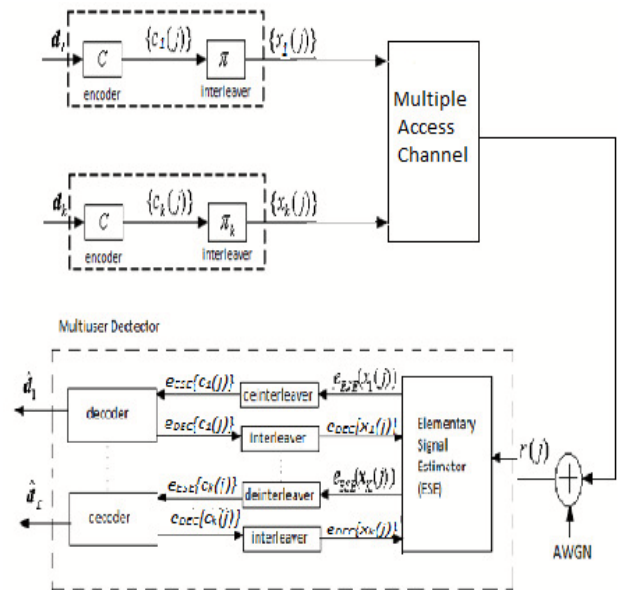
II. IDMA SYSTEM MODEL

Figure: 1 IDMA System Model

IDMA is a multiple access technology with chip-level interleaving and iterative detection. Figure 1 shows the model of IDMA system. The input data sequence d_k of user-k is encoded based on a low rate code C, generating a coded sequence.

$C_k = [C_k(1),\ldots\ldots, C_k(j),\ldots\ldots, C_k(J)]$, where J is the length of coded sequence. Then C_k is permutated by an interleaver π_k, producing $x_k = [x_k(1),\ldots\ldots, x_k(j),\ldots\ldots, x_k(J)]$.

We assume the channel without memory, so the received signal from K users can be written as:

$$r(j) = \sum_{k=1}^{K} h_k x_k(j) + n(j), \ j=1,2,\ldots\ldots,J. \tag{1}$$

Where h_k are the channel coefficient and n(j) are the samples of AWGN noise with variance $\sigma^2 = N_0/2$.

We can rewrite (1) as:

$$r(j) = h_k x_k(j) + \zeta_k(j), \tag{2}$$

where $\quad \zeta_k(j) = r(j) - h_k x_k(j) = \sum_{k' \neq k} h_{k'} \cdot x_{k'}(j) + n(j). \tag{3}$

From the central limit theorem $\zeta_k(j)$ can be approximated as Gaussian variable. So

$$P(x_k(j) = +1 | r(j)) = \frac{1}{\sqrt{2\pi Var(\zeta k(j))}} \exp \frac{r(j) - ((\pm h k + E((\zeta \kappa (j)))^2}{2Var((\zeta k(j))} \tag{4}$$

We define output of the elementary signal estimator (ESE) as:

$$e_{ESE}(x_k(j)) = \log\left(\frac{p(xk(j) = +1|r)}{p(xk(j) = +1|r)}\right), \forall k,j. \tag{5}$$

Then

$$e_{ESE}(x_k(j)) = 2h_k\left(\frac{r(j) - E(xk(j))}{Var(\zeta k(j))}\right). \tag{6}$$

The decoder (DEC) detection carries out a posteriori probability (APP) decoding using the output of the ESE as the input.

$$e_{DEC}(x_k(j)) = \log\left(\frac{p(xk(j) = +1|r)}{p(xk(j) = +1|r)}\right), \forall k,j. \tag{7}$$

There r is formed by the deinterleaved version of the output of the ESE. We use the e_{DEC} to generate the following statistics:

$$E(x_k(j)) = \tanh(e_{DEC}(x_k(j))/2) \tag{8}$$

$$Var(x_k(j)) = 1 - (E(x_k(j)))^2 \tag{9}$$

In the next iteration, the statistics (8) (9) are used to refresh the ESE.

III. INTERLEAVING TECHNIQUES

A. Random interleaver

Random Interleavers are generated independently and randomly. Random interleavers for IDMA need to satisfy two design criteria [16]

1) They are easy to specify and generate, i.e., the transmitter and receiver can send a small number of bits between each other in order to agree upon an interleaver, and then generate it.

2) The interleavers do not "collide".

The collision among interleavers is interpreted in the form of the uncorrelation among the interleavers. If the interleavers are not randomly generated, the system performance degrades considerably and the MUD is unable to resolve MAI problem at the receiver resulting in higher values of Bit Error Ratio (BER). On the other hand if the interleaving patterns are generated more and more random, the MUD resolves the MAI

problem more quickly and better values of BER are obtained for the same parameters.

B. Power interleaver

In an IDMA scheme, each user has a user specific interleaver $\{\pi_k\}$ having length equal to chip length 'J'. Therefore, a considerable amount of memory will be required to store the indexes for these interleavers. In power interleavers [7] a master interleaver φ (say) is chosen. Then the K interleavers can be generated using $\pi_k = \varphi^k$. Here, $\varphi^k(c)$ is defined as $\varphi^1(c) = \varphi(c)$, $\varphi^2(c) = \varphi(\varphi(c))$, $\varphi^3(c) = \varphi(\varphi(\varphi(c)))$, etc. In this way, every interleaver is a power of φ. The rationale for this method is that if φ is an 'ideal' random permutation, so are all $\{\varphi^k\}$, and these permutations are also approximately independent to each other. Based on this method, we simply assume that the base station (BS) assigns the power index k to each user k, and then φ^k will be generated at the mobile station (MS) for user k accordingly.

C. Tree based interleaver

The Tree Based Interleaver is basically aimed to minimize the computational complexity and memory requirement that occurs in power interleaver and random interleavers respectively. In a Tree Based Interleaver generation, two randomly generated interleavers are chosen; let π_1 and π_2 are the two randomly selected interleavers. These interleavers are tested to have zero cross correlation between each other. The combinations of these two interleavers in a particular manner [8] are used as interleaving masks for the users. The allocations of the interleaving masks follow the tree format. The Tree Based Interleaving scheme reduces the computational complexity that occurs in the power interleaving scheme. The mechanism involved in generation of tree based user specific interleavers is shown in figure 2. The two randomly selected interleavers are solely responsible for generation of other interleavers related to other users.
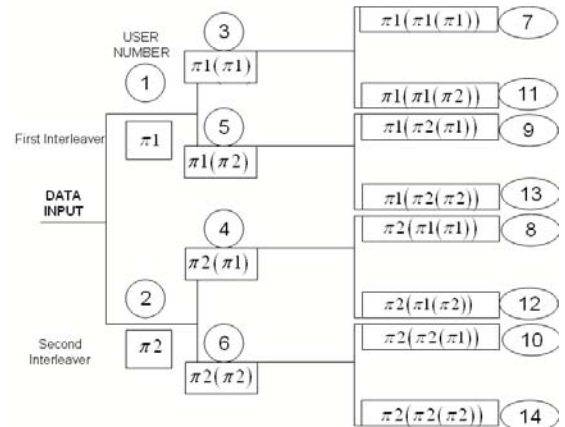

Figure: 2 interleaving mask allocation for tree based interleaver.

D. Shifting interleaver

Shifting interleaver can be generated with one primitive polynomial of degree m for any interleaving length N. For

large scale IDMA system where user number K is large, it is difficult to find enough primitive polynomials for pseudo-random interleavers, and system have to tolerate generation time for nested interleavers [6], shifting interleavers become useful for large scale IDMA system. Shifting interleaver can be described as a two stage, generating π_{master} and shifting described as follows

Stage 1: generating π_{master}

1) Assign a storage S with length N.

2) Initialize the PN sequence generator with p_k {$p_k \in GF(2)$, $1 \leq k \leq m$} and mark this state as $state_1$.

3) Update the state of the PN sequence generator with p_k, after the nth ($1 \leq n \leq m$) update, mark the state as $state_n$.

4) If $state_n \leq N$, put it in S, then return 3), otherwise, return 3).

5) If S is full, the update is terminated.

Through this method, the states stored in S will be the π_{master}.

Stage 2: shifting

π_k, the interleaver of user k, is generated by circular shifting L×k steps of the π_{master}.

$\pi_k = f(\pi_{master}, L \times k)$, $1 \leq k \leq K$. Where L=int(N/K) is the unit step of shifting. int(x) returns the greatest integer that is not larger than x, N is the length of interleaver and K is the total number of users. According to the characteristics of the PN sequence, these K interleaving addresses are less correlated. Thus these shifting sequences can be used as interleaving addresses for different users in the IDMA systems. An example of shifting interleaver generation is given in [9].

E. 2-Dimension interleaver

In [9] we can achieve same performance comparing to random interleaver with much fewer resources. But the problem for shifting interleavers is that we have to search high order primitive polynomial for large N. 2-Dimension interleavers [10],developed to overcome this problem, which can generate a long sequence by utilizing a much lower order primitive polynomial. 2-Dimension interleavers can be described as a two stage, generating π_{master} and shifting. Before generating π_{master} an interleaver Γ is generated according to the algorithm described above for the generation of π_{master} for shifting interleaver.

Stage 1: generating π_{master}

Assume a matrix $M_{nxn}(n > N^{1/2})$ and the indices$\{1,2,3...n^2\}$ are written into M_{nxn} by rows. We assume an interleaver Γ with length n. before we read out the indices by columns we scramble the row indices and column indices successively with Γ.

Stage 2: shifting

π_k, the interleaver of user k, is generated by circular shifting L×k steps of the π_{master}.

$\pi_k = f(\pi_{master}, L \times k)$, $1 \leq k \leq K$. Where L=int(N/K) is the unit step of shifting. int(x) returns the greatest integer that is not larger than x, N is the length of interleaver and K is the total number of users [10].

F. Parallel interleaver

The receiver of IDMA systems adopts iterative MUD described in [11]. So far, both of the interleaving and de-interleaving operations permute sequences serially, which will take many hardware clock periods and lead to much processing latency and low processing throughput. This has been the bottleneck of the system throughput, especially when the iteration numbers are large. The memory access conflict may appear during the exchange of extrinsic information between the DEC and ESE. Shuang Wu et al [12] proposed the concept of parallel interleaver to overcome memory access conflict, this means that two or more processors try to access the data in the same memory unit simultaneously, which may have a severe impact on the receiver performance.

Below, the main design principles of the parallel interleavers will be presented. Let us define the following parameters:

N number of chips in a frame

D number of information bits per frame per user

M degree of parallel processing

W number of chips to be processed in each processor

Here, N = DS = MW and W are constrained. For example, with linear block codes, W is an integer multiple of the coding length, and with repetition codes, W is an integer multiple of the spreading length S. The algorithm for the parallel interleaver design, can be divided into five stages, which are given as

Stage 1: Assign the initial matrices with M rows and W columns.

Stage 2: Put the coded bits into matrices by rows.

Stage 3: Perform column-wise interleaving for each column.

Stage 4: Perform row-wise interleaving for each row.

Stage 5: Read out the bits by rows.

Detailed descriptions of Stage 3 and 4 are given as follows

Stage 3: column permutation

1) Different random seeds are allocated to different users.

2) For user k, independent random sequences with length M are generated by its own random seed.

Stage 4: row permutation

1) Let π_{ini} be the initial interleaver with length W.

2) π_k, the interleaver of the first row of user k, is generated by cyclically shifting the initial interleaver by Lk steps, where

L = int(W/K) , and int(x) returns the greatest integer that is no larger than x.

3) For user k, the interleaving patterns of the following row are generated by cyclically shifting the previous row's interleaver one step.

G. Prime number based interleaver

In IDMA, different users are assigned different interleavers which are weakly correlated [6]. The computational complexity and memory requirement should be small for generation of interleavers. The Prime Interleaver proposed by Ruchir Gupta et al[15] is basically aimed to minimize the bandwidth and memory requirement that occur in other available interleavers with bit error rate (BER) performance comparable to random interleaver. In generation of prime interleaver we have used the prime numbers as seed of interleaver. Here, user-specific seeds are assigned to different users.

For understanding the mechanism of prime interleaver, let us consider a case of interleaving n bits with seed p. First, we consider a Gallois Field GF (n). Now, the bits are interleaved with a distance of seed over GF (n). In case, if {1, 2, 3, 5, 6, 7, 8… n} are consecutive bits to be interleaved with seed p then location of bits after interleaving will be as follows:

1===> 1

2===> (1+p) mod n

3===> (1+2p) mod n

4===> (1+3p) mod n

. ..

n===> (1+(n-1)p) mod n

H. Linear congruential interleaver

This interleaver design for IDMA is based on linear congruences [13] [14]. In this scheme, a seed interleaver $\square_{seed}$ can first be generated by the linear congruence method. The purpose of the seed interleaver is to maintain low correlation among interleavers. Afterwards, the interleavers for the users from the seed interleaver $\square_{seed}$ using algorithm based on linear congruences [13] are derived. Less amount of memory is required for storing the interleavers in linear congruential interleaver than in the pseudo random interleaver design. Let different interleaving patterns for different users be represented by ICRSk(j), j = 0,1, ... , p-1 , where k denotes an interleaver for the kth user and p is the length of the interleaver. For a particular k, The linear congruence theorem [13] guarantees that {ICRSk (j),j =0, I, ..., p-I} does not have any repeated number.

IV. PERFORMANCE ANALYSIS

A. Performance of different interleavers in uncoded environment

In this section we will show the performance of different interleavers for uncoded IDMA system. For simplicity, IDMA

system with BPSK signaling in AWGN channel for h_k=1, $\forall$ k is assumed. Without loss of generality, a uniform repetition coding {+1,-1, +1,-1,…..} is used for all users. For random interleaver performance criterion of [16] is taken, power interleaver performance is based on [7], tree based interleaver performance is based on the performance criterion given in [8], shifting interleaver performance is based on [9], 2-D interleaver performance is analyzed by using [10] simulation criterion, parallel interleaver performance is given according to [12] [6], prime no based interleaver performance is based on [15], linear congruential interleaver is analyzed based on [14]. Figures 3-9 show the performance of different interleavers described in previous section. In which x-axis represents energy per bit to noise power spectral density ratio (Eb/N0), and y-axis represents bit error rate (BER).
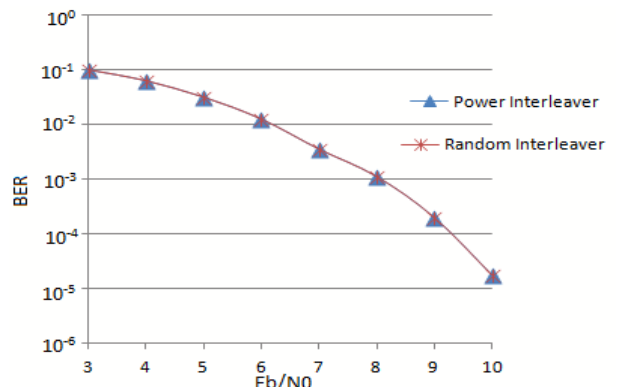

Figure: 3 Performance results for uncoded IDMA systems. Iteration number=20.
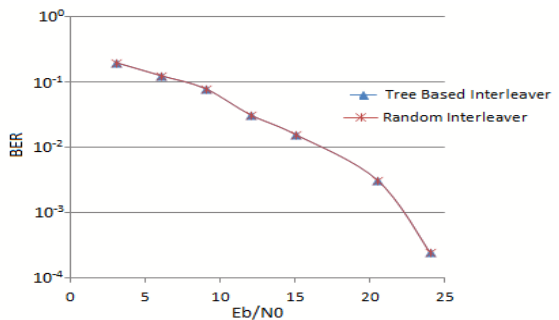

Figure: 4 Performance results for uncoded IDMA systems. Iteration number=15.
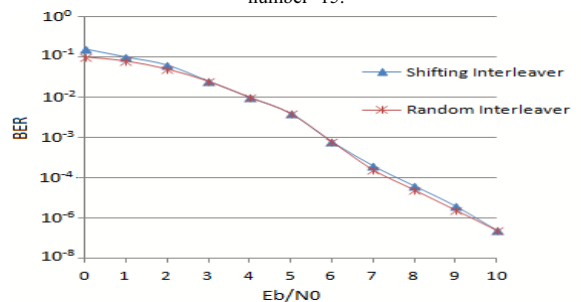

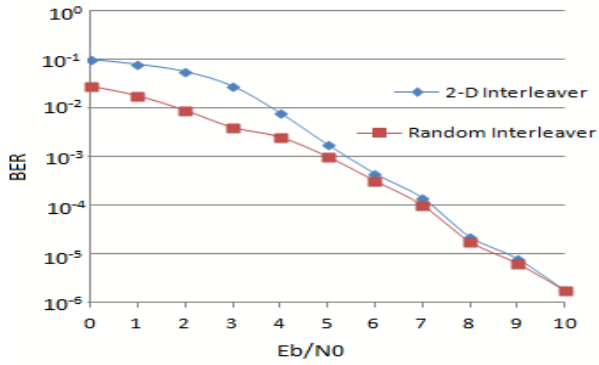Figure: 5 Performance results for uncoded IDMA systems. Iteration number=20.

Figure: 6 Performance results for uncoded IDMA systems. Iteration number=5.
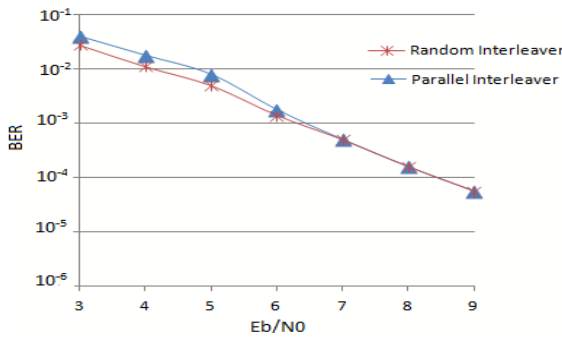

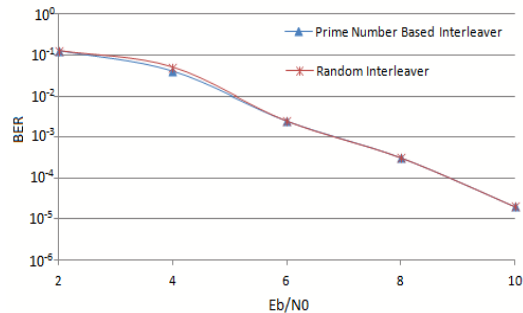Figure: 7 Performance results for uncoded IDMA systems. Iteration number=10.

Figure: 8 Performance results for uncoded IDMA systems. Iteration number=15.
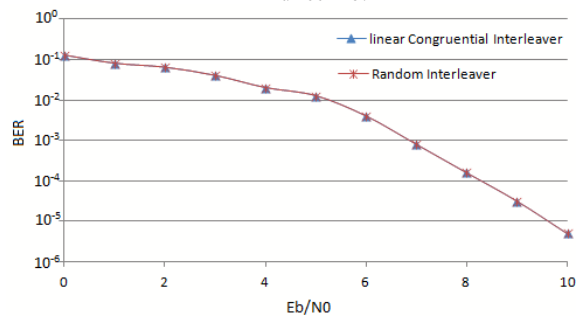

Figure: 9 Performance results for uncoded IDMA systems. Iteration number=5.

B. Convolutional coded system performance

For the performance of coded IDMA system convolutional code was implemented, generating output code bits at a rate of ½. Figures 10-12 show the performance of convolutional coded IDMA systems with respect to Random Interleaver.
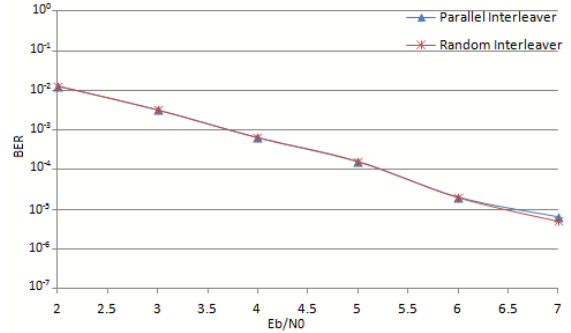

Figure: 10 Performance results for convolutional coded IDMA systems, with generator polynomial $(7, 5)_8$. Iteration number=10. Users=16.
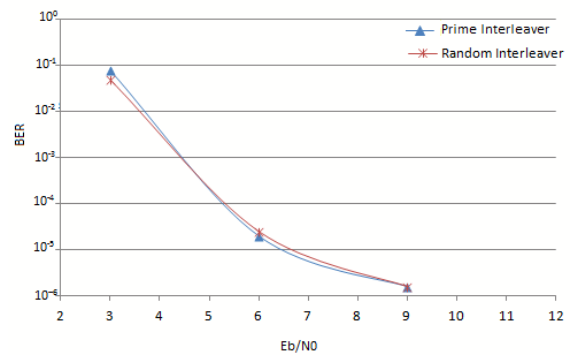

Figure: 11 Performance results for convolutional coded IDMA systems. Iteration number=15. Users=16.
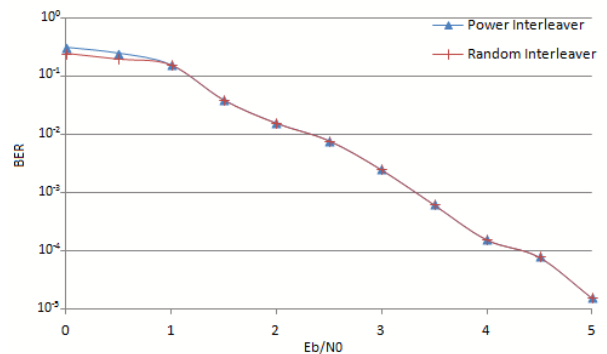

Figure: 12 Performance results for convolutional coded IDMA systems, with generator polynomial $(23, 35)_8$. Iteration number=20. Users=16.

C. Comparison table

Table I: Table for the comparison of some important parameters

Parameters/ Interleavers	Memory/B.W. Consumption	Computational Complexity
Power interleaver(POI)	Lower than SI	High
Tree based interleaver (TBI)	More than POI	Lower than PNBI
Shifting interleaver(SI)	More than POI	Lower than POI
2-dimension interleaver (2-DI)	Less than SI	Lower than SI
Parallel interleaver (PI)	Very low memory requirement	Very low
Prime no. based interleaver (PNBI)	Lower than TBI	Lower than POI
Linear congruential interleaver (LCI)	Lower than random interleaver(RI)	low

V. CONCLUSION

In this paper, we have reviewed the performances of different interleavers with respect to random interleaver. The computational complexity of power interleaver is the highest and that of parallel interleaver is the lowest, and memory requirement is the lowest for parallel interleaver among all the interleavers given in this paper. The Bit Error Rate (BER) performance of all the interleavers is very similar to that of the random interleavers. Parallel interleavers, prime number based interleavers and power interleavers give very similar BER performance to that of random interleavers in coded environment.

In future we will find the performance of interleavers given in this paper for various coding schemes.

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