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Design and Performance Comparison of 7-level Diode Clamped Multilevel Inverter for Modified SVPWM Techniques

[Ch. Lokeshwar Reddy, P. Satish Kumar, M. Sushama]

***Abstract*—In this paper, a 7-level Diode Clamped Multilevel Inverter (DCMLI) is simulated with three different carrier PWM techniques. Here, Carrier based Sinusoidal Pulse Width Modulation (SPWM), Third Harmonic Injected Pulse Width Modulation (THIPWM) and Modified Carrier-Based Space Vector Pulse Width Modulation (SVPWM) are used as modulation strategies. These modulation strategies include Phase Disposition technique (PD), Phase Opposition Disposition technique (POD), and Alternate Phase Opposition Disposition technique (APOD). In all the modulation strategies triangular carrier and trapezoidal triangular carrier signals are compared with reference signal and control pulses are generated. The detailed analysis of the results has been presented and studied in terms of fundamental component of output voltage and THD.**

***Keywords*—DCMLI, PDSVPWM, PODSVPWM, APODSVPWM.**

I. Introduction

Multilevel inverter structures are most popular for high power applications, since the harmonics in the output voltage significantly condensed by using several voltage levels whereas switching at the same frequency. The switches are connected in series for the multilevel inverters, then higher input DC voltages can be used and this reduces the withstand DC voltages for each device.

Multilevel inverters are mainly formulated for high power applications, owing to higher voltage working ability, lower dv/dts and reduced harmonics in the outputs. In recent years, industry has started to demand high power equipment's, now these spread to megawatt level. In megawatt range the controlled ac drives are typically connected to the medium-voltage network [1]. It is difficult to connect a single power semiconductor switch to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV) directly. Due to these reasons, multilevel inverters have been developed as the solution for working with higher voltage levels.

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In this paper a 7-level diode clamped inverter is simulated with three different modulation techniques and detailed analysis of the results has been presented.

II. Diode Clamped Multilevel Inverter

The Diode Clamped Multilevel Inverter (DCMLI) uses a single dc bus which is further divided into a number of voltage levels using a series string of capacitors. Each active switching device is only required for blocking a voltage level of Vdc/(m-1) where m is number of levels, but the clamping diodes must have different voltage ratings to block the reverse voltage[2]. The number of diodes essential for each phase will be (m-1) *(m-2). This number indicates a quadratic increase in m. When the number of levels goes on increasing, the number of diodes increases making the system impractical to implement.

To run the inverter with PWM, the reverse recovery of clamping diodes becomes the major problem while designing for high-voltage and high-power applications. Fig 1. shows the model for 7-level diode clamped inverter.

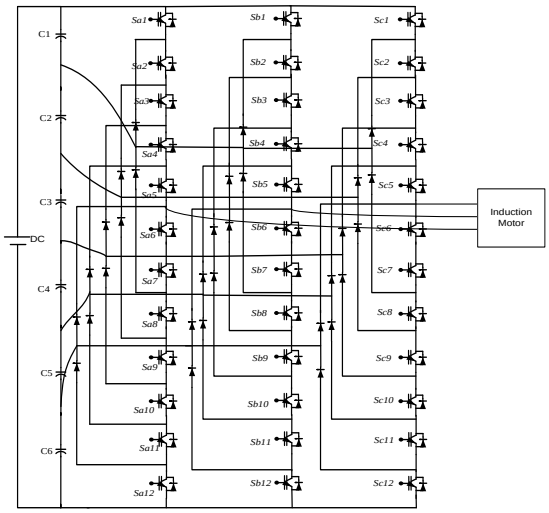

Figure 1. 7-level Diode Clamped Multilevel Inverter

III. Multi Carrier SPWM Techniques

Modulation techniques for multilevel inverters are based on carrier arrangements. The carriers shifted horizontally is Phase Shifted Carrier PWM (PSCPWM). Generally, this technique is preferred for the CMLI, the implementation is

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easy and it distributes power evenly among all the cells [3]. This technique results in the termination of all carrier and associated sideband harmonics up to $2N^{th}$ carrier group, where N is the number of H-bridges in each phase [4]. To implement easily on digital controller, vertical shifted carrier techniques are preferred. This scheme consists of three different techniques

1. All carrier signals are in Phase (Phase Disposition-PD)
2. Half of the carrier signals above are in same phase and half below carriers are in same phase but the phase difference between these two half's is180^0(Phase Opposition Disposition- POD)
3. All carriers are alternatively in opposition (Alternate Phase Opposition Disposition – APOD)

The switching frequency will be high, to reduce the undesired side effects of irregular power flow at switching and to ease lower harmonics in the output voltage.

The fundamental reference waveform of individual phase with the addition of common mode third-harmonic term increases the modulation index of a three phase inverter. As the common voltages neutralize among the phase legs, the third harmonic component has no influence on the line to line fundamental output voltage, but it reduces the maximum value of each phase leg voltage. Therefore, the modulation index can be amplified without entering into over modulation.

With the magnitude 1/6 of third harmonic injected waveform and 1.15 of fundamental waveform the reference waveform magnitude is increased. The reference voltages for Third Harmonic Injected Phase Shifted Carrier (THIPSC) technique are

$$V_a(t) = 1.15\sin(wt) + (1/6)\sin(3wt) \quad (1)$$

$$V_b(t) = 1.15\sin(wt - 2*pi/3) + (1/6)\sin(3wt) \quad (2)$$

$$V_c(t) = 1.15\sin(wt - 4*pi/3) + (1/6)\sin(3wt) \quad (3)$$

IV. Modified Carrier-Based SVPWM

In conventional SVPWM the mapping of the outer sectors to an inner sub hexagon sector should be done in order to determine the switching time duration for multilevel inverters. The switching vectors equivalent to the existing sectors are switched and the time periods calculated from the mapped inner sectors. Due to the presence of high number of sectors and inverter sectors realizing this technique will be difficult in multilevel inverters. And computation time is raised in this method during real time applications.

Before comparing with carrier waves, sinusoidal references are included with proper offset voltage to reach the performance of SVPWM in carrier based PWM technique [5]. The calculation of offset voltage is depending on modulus function which depends on the DC link voltage, number of levels and the phase voltage magnitudes.

Another modulation technique is provided in which sinusoidal reference phase voltages are included with common mode voltage of appropriate magnitude all through the interval [6]. Addition of common mode voltage will not give same performance of SVPWM, because middle inverter vectors will not be centered in a sampling interval [7]. Another modulation technique is provided in [8], where a fixed common mode voltage is included with the reference phase voltage all through the modulation range.

A simplified method presented, where correct offset times are determined for centering the time durations of middle inverter vectors in a sampling interval. A procedure is given in [9] for finding the maximum probable peak amplitude of the fundamental phase voltage in the linear modulation. The following equations are used to calculate offset time $T_{offset.}$

$$T_a = \frac{V_a * T_s}{V_{dc}} \quad (4)$$

$$T_b = \frac{V_b * T_s}{V_{dc}} \quad (5)$$

$$T_c = \frac{V_c * T_s}{V_{dc}} \quad (6)$$

Where Ta, Tb and Tc are the time periods of imaginary switching, proportional to the instantaneous values of the reference phase voltages V_a, V_b and V_c and Ts is the sampling time period.

$$T_{offset} = [\frac{T_0}{2} - T_{\min}] \quad (7)$$

$$T_0 = [T_s - T_{effect}] \quad (8)$$

$$T_{effect} = T_{\max} - T_{\min} \quad (9)$$

T_{max} = Maximum magnitude of the three reference phase voltages, in a sampling interval.
T_{min} = Minimum magnitude of the three reference phase voltages, in a sampling interval.

The inverter switching vectors are centered in a sampling interval by the addition of offset voltage to the reference phase voltages that equate the performance of SPWM technique with the SVPWM technique [10].

This proposed SVPWM signal generation does not involve look up table, sector identification, angle information and voltage space vector amplitude measurement for switching vector determination required in the conventional multilevel SVPWM technique. This scheme is more effective when compared with conventional multilevel SVPWM technique. Fig. 3 shows the generated there-phase reference waveforms by the modified SVPWM technique. These reference waveforms are compared with triangular and trapezoidal triangular carriers to generate gate pulses for the switching devices. Fig. 4 shows the

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comparison between the reference waveforms generated by modified SVPWM and third harmonic injected techniques.

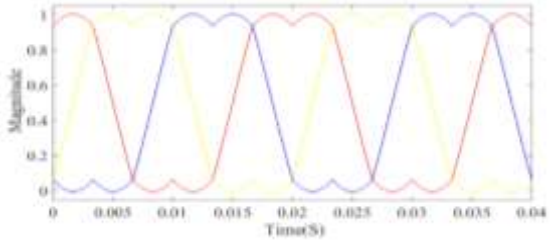


Figure 3. Reference signals for Modified SVPWM

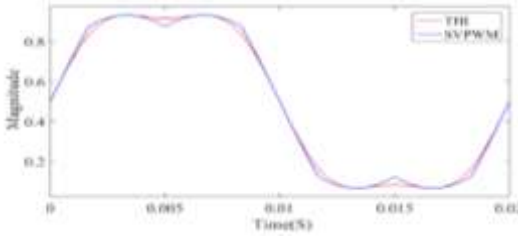
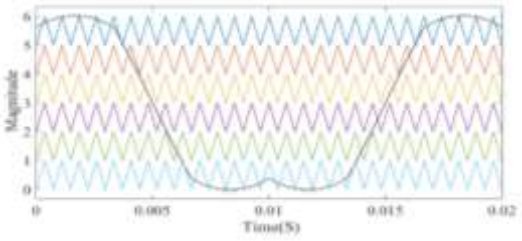
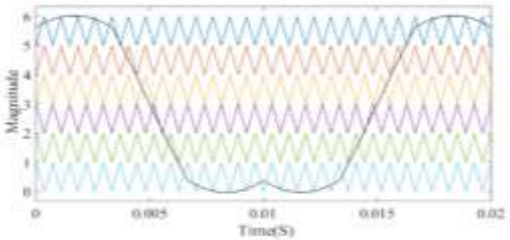


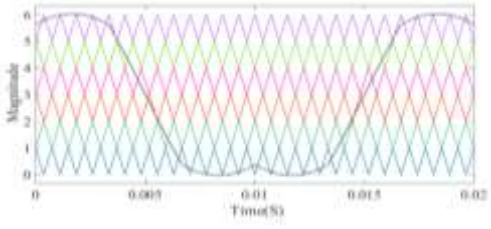
Figure 4. Comparison between reference signals of THI and Modified SVPWM



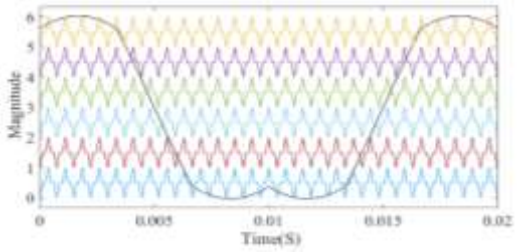
a) PDSVPWM



b) PODSVPWM



c) APODSVPWM



d) PDSVPWM- Trapezoidal

Figure 5. Different Modified SVPWM techniques

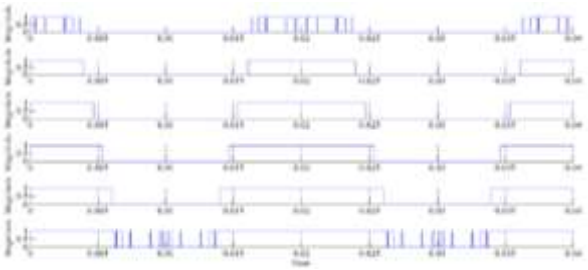


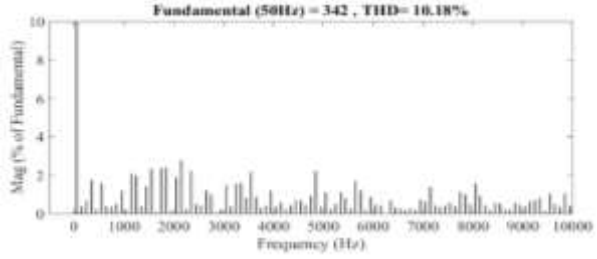
Figure 6. Gate pulses for SVPWM technique

Fig. 5 shows the comparison of reference waveform generated by modified SVPWM technique with level shifted triangular carrier waveforms to generate gate pulses for the switching devices. Fig. 6 shows the gate pulses generated by PDSVPWM technique, it is observed that the active switching pulses are centered in a sampling interval, then this equates the performance with conventional SVPWM technique.

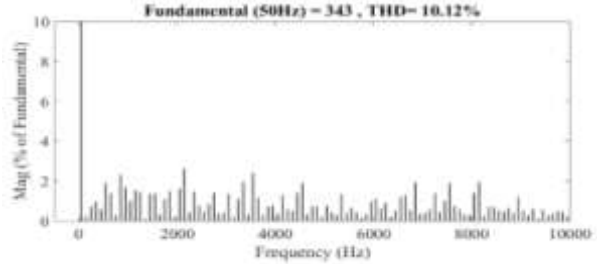
v. Simulation Results and Discussion

Simulations are carried out using Matlab/Simulink environment for the 7-level DCMLI and the CMLI by implementing SPWM, THIPWM and Modified SVPWM techniques. A 3-phase induction motor is considered as load for this scheme. Single DC voltage source of 400 V is connected to the DCMLI and separate DC voltage sources are set to 133 V for each H-bridge that is connected to CMLI.

Fig. 7 shows the harmonic analysis of DCMLI for different SPWM techniques with triangular as carrier wave for all the techniques and trapezoidal triangular as carrier for the PDSPWM technique. The fundamental component in all the techniques is the same. The PDSPWM with trapezoidal triangular carrier gives better harmonic performance to the other SPWM techniques.



a) PDSPWM



b) PDSPWM-Trapezoidal

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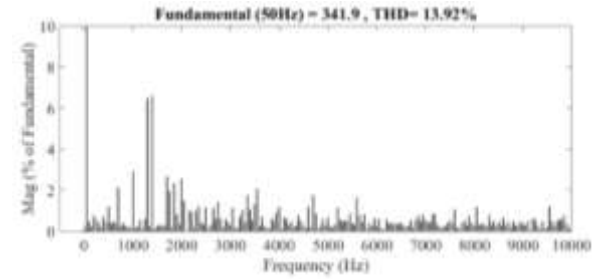
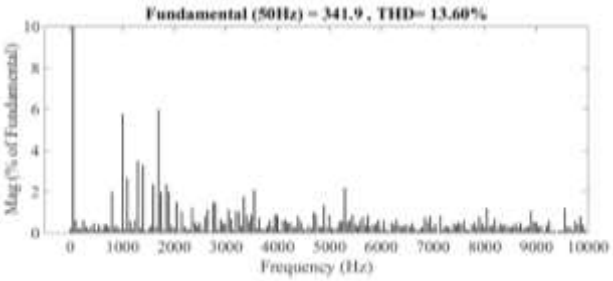


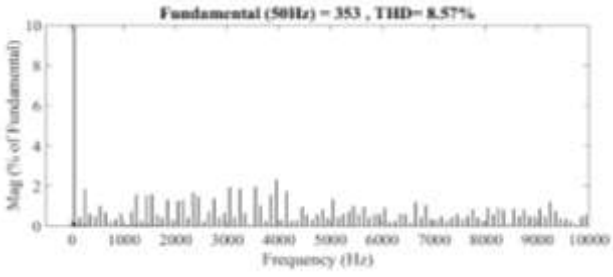
c) PODSPWM



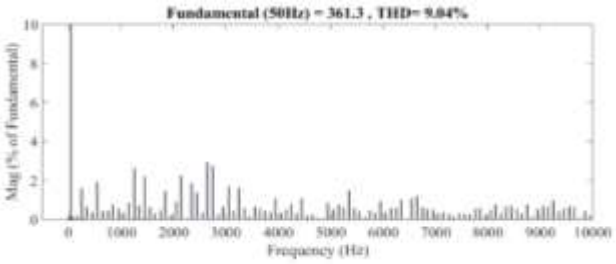
d) APODSPWM

Figure 7. Harmonic analysis of DCMLI for different SPWM techniques

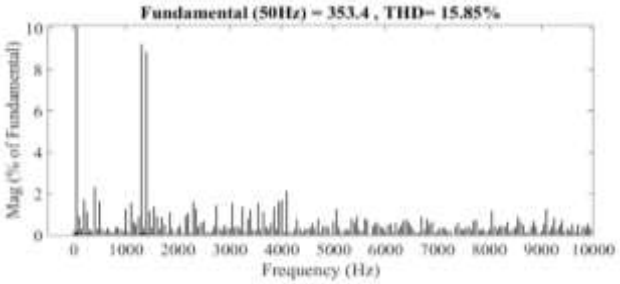
Fig. 8 shows the harmonic analysis of DCMLI for different THI techniques with triangular as carrier wave for all the techniques and trapezoidal triangular as carrier for the PDTHI technique. The fundamental component in all the techniques is the same but the PDTHI with trapezoidal triangular technique produces more. The utilization of DC link is almost 3% more in the THI technique with triangular carrier and is 6% more with trapezoidal triangular carrier wave with respect to the SPWM techniques. The PDTHI with triangular carrier gives 8.57% of THD, which is better harmonic performance to the other THI techniques.



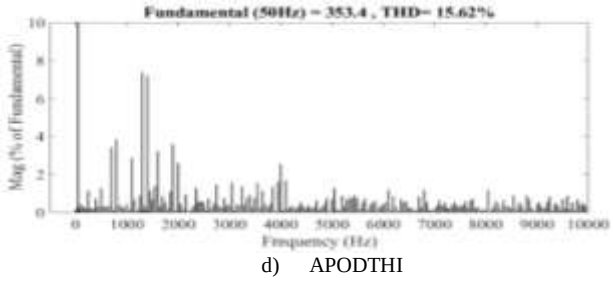
a) PDTHI



b) PDTHI- Trapezoidal



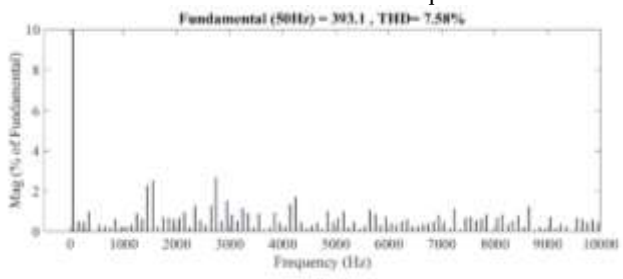
c) PODTHI



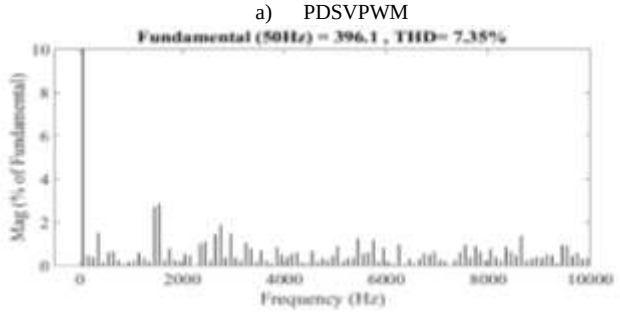
d) APODTHI

Figure 8. Harmonic analysis of DCMLI for different THIPWM techniques

Fig. 9 shows the harmonic analysis of DCMLI for different modified SVPWM techniques with triangular as carrier wave for all the techniques and trapezoidal triangular as carrier for the PDSVPWM technique. The fundamental component in the PDSVPWM and the APODSVPWM techniques is the same but the PDSVPWM with trapezoidal triangular carrier technique produces more and the PODSVPWM technique produces less. The utilization of DC link is almost 15% more in the SVPWM technique with triangular carrier and is around 16% more with trapezoidal triangular carrier wave with respect to the SPWM techniques. The PDSVPWM with trapezoidal triangular carrier gives 7.35% of the THD, which is better harmonic performance to the other SVPWM techniques.



a) PDSVPWM



b) PDSVPWM-Trapezoidal

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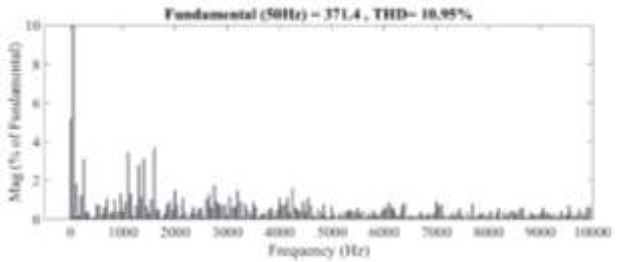
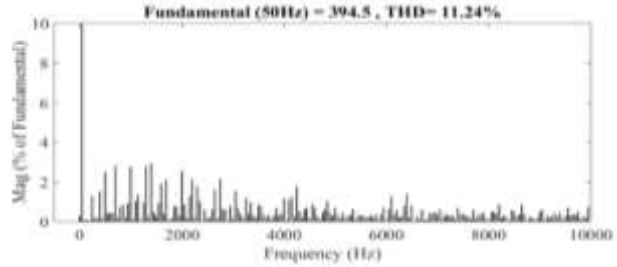


c) PODSVPWM



d) APODSVPWM

Figure 9. Harmonic analysis of DCMLI for different SVPWM techniques

The table. 1 gives the performance comparison of a 7-level Diode clamped inverter for different Sinusoidal, Third Harmonic injected and Space vector PWM techniques. The performance of the Diode clamped inverters for POD and APOD are almost similar for all the three modulation techniques in terms of %THD. The utilization of DC link voltage is almost 15% more in SVPWM technique and 3% more in THIPWM with respect to the SPWM technique for triangular carrier wave and it is further more for trapezoidal triangular carrier wave. The % THD is approximately the same for both the carrier waves.

VI. Conclusion

In this paper new multicarrier SVPWM techniques such as Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD) have been implemented for 7-level DCMLI. These results are compared among each other. It is observed that PDSVPWM technique with Trapezoidal Triangular carrier gives 7.35 % of THD, which is better performance with respect to other techniques. The utilization of DC link is almost 15% more in the SVPWM technique with triangular carrier and is around 16% more with trapezoidal triangular carrier wave with respect to the SPWM techniques. The performance of the Diode clamped inverters for POD and APOD are almost similar for all the three modulation techniques in terms of %THD.

TABLE I. PERFORMANCE COMPARISON OF DCMLI

	SPWM		THIPWM		SVPWM	
	Fundamental Component	**% THD**	**Fundamental Component**	**% THD**	**Fundamental Component**	**% THD**
PD	342	10.18	353	8.57	393.1	7.58
PD (Trapezoidal Triangular Carrier)	343	10.12	361.3	9.04	396.1	7.35
POD	341.9	13.92	353.4	15.85	371.4	10.95
APOD	341.9	13.60	353.4	15.62	394.5	11.24

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