

Design and Implementation of MIL-STD-1553B RT Subsystem

[Seung-Han Kim, Chang-Hoon Cho, Dong-Seong Kim*, and Jae-Min Lee]

Abstract— In this paper, the MIL-STD-1553B RT(Remote Terminal) subsystem based on FPGA and IP Core was implemented. Proposed system integrate CPU, ASIC, and peripheral circuits of the MIL-STD-1553B system on one chip. Through this, scalability of the MIL-STD-1553B system can be enhanced. For verifying proposed FPGA based the MIL-STD-1553B system, simulation environment was constructed with the MIL-STD-1553B tester and test software for identifying electrical characteristics and data communication functions. Simulation results show that proposed system can be interfaced with the MIL-STD-1553B data bus and advantageous in manufacturing cost reduction because of its scalability.

Keywords— MIL-STD-1553B, FPGA, IP Core, Real-time System.

I. Introduction

The MIL-STD-1553, one of the military fieldbus standard, is adopted in military and aerospace craft because of its reliability and real-time property[1][2]. Especially in military networks, the MIL-STD-1553B is used for developing real-time system[3]. The MIL-STD-1553B subsystems, included in aircraft, are increased and become complicate in recent year. But most of the MIL-STD-1553B equipments are expensive and support limited interfaces such as PCI or PCMCIA. Thus, lacks of scalability of the MIL-STD-1553B equipment cause rise of its costs. Especially, the development and managing of the MID-STD-1553B system has difficult problem because of its cost and technology dependability[4-7]. In recent day, some of the MIL-STD-1553B devices which supports USB or Ethernet interface are released, but these modules are also expensive. To solve these problems, an IP Core based the MIL-STD-1553B controller was implemented in research[8][9] and a FPGA based the MIL-STD-1553B controller was implemented in [10]. These researches can reduce cost of the MIL-STD-1553B because of its scalability and reusability. But one-chip based the MIL-STD-1553B RT(Remote Terminal) subsystem is not implemented in these researches.

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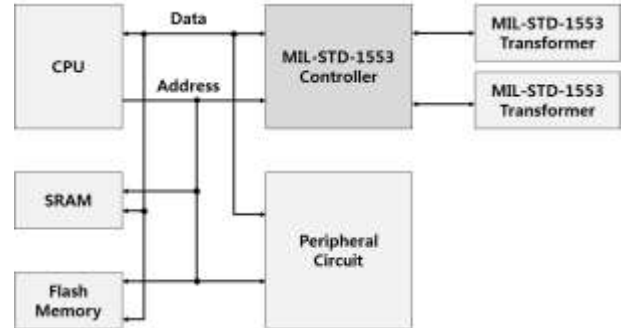


Figure 1. Configuration of Existing Subsystem of MIL-STD-1553B.

The configuration of the existing MIL-STD-1553B subsystem is shown in Fig. 1. In the existing MIL-STD-1553B subsystem, most of the components are installed independently. But, the proposed system, most of the components are implemented in one chip, can minimize design space and reduce implementation costs. The most of the functions of RT subsystem for interfacing with the MIL-STD-1553B data bus are implemented on one-chip in proposed system. In simulations, the MIL-STD-1553 Bus Tester, USB Type, and software for development and verification were used for verifying performance of proposed system.

The composition of this paper is as follows. In section II, design and implementation of proposed system were described. In section III, we evaluate and analyze performance of proposed system. In section IV, we discuss about conclusion and future work.

II. FPGA based MIL-STD-1553B RT Subsystem

In this paper, CPU IP Core and controller IP Core of the MIL-STD-1553B were installed on FPGA to implement the MIL-STD-1553B RT-specific subsystem. Through this, density of design is enhanced and technology dependence is reduced. The overall design of proposed system is shown in Fig. 2.

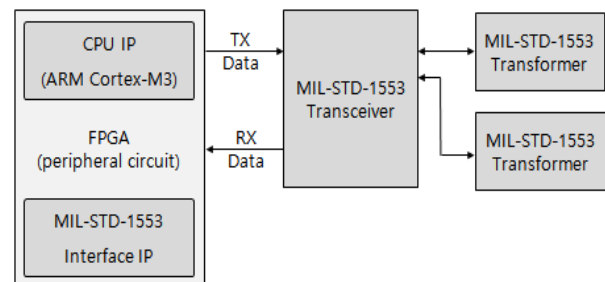


Figure 2. FPGA based Subsystem Control Module.

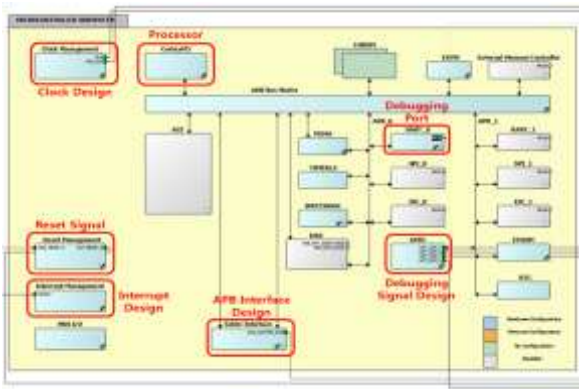


Figure 3. Detail of FPGA based Subsystem Control Module.

In this research, Core1553BRT_APB is chosen as the MIL-STD-1553B controller IP Core and Coretex™-M3 is selected as CPU IP Core[11]. Using Core1553BRT_APB, RT-specific IP Core, the system implementation cost can be reduced by excluding the unused logic of BC(Bus Controller) and BM(Bus Monitoring) protocol. The Coretex™-M3 provides high performance and low cost and it is interfaced to AMBA(Advanced Microcontroller Bus Architecture). For integration of these modules, we selected A2F200 series in FPGA device. Function blocks of the selected FPGA device are divided by a processor block, an FPGA block, and an analog circuit block. IP Core and user custom logic can be installed on each function block through development software. We can implement user custom logic on function block which is not installed IP Core in FPGA. In this paper, we design logic to connect with the MIL-STD-1553B data bus. Detail design and implementation of the system are as follows:

The selected FPGA device provides a MSS(Microcontroller SubSystem) that includes Coretex™_M3 IP Core, Ethernet MAC, and etc. To install MSS block on FPGA, Libero SoC software tool is used in this research. The design of the MIL-STD-1553B RT subsystem in Libero SoC software is shown in Fig. 3.

After placing Coretex™-M3 on canvas, we install Core1553BRT_APB on canvas and then set option of port on Core1553BRT_APB. Table I describe port option of Core1553BRT_APB.

TABLE I. CORE1553B_APB PORT SETTING

Port	Variable Setting
RTADDR[4:0]	5Bit RT Address Input
RTADERR	RT Address Odd Parity Input
RTADDRP	RT Parity Error Output
BUSAINEN	BUS A I/O and Activate Signal
BUSAINP	
BUSAINN	
RSTINn	Asynchronous Reset Signal Input
RESETN	
CMDVAL[11:0]	Command Word, Broadcast Status Information
CMDSTB	CMDVAL Change Status Signal Output
CMDOKAY	CMDVAL Idle Status Signal Output

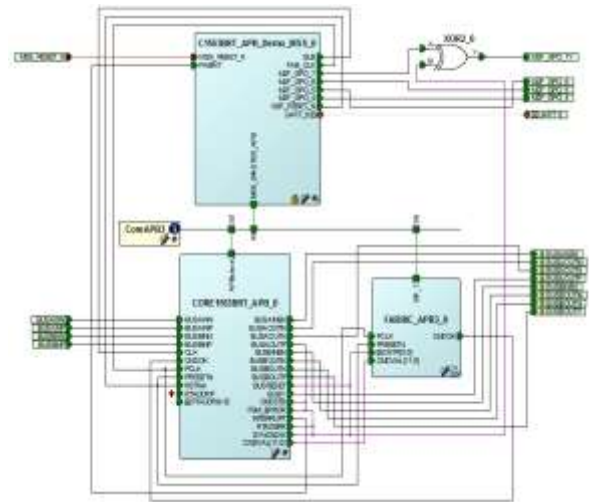


Figure 4. Routing of Functional Block on Designed MIL-STD-1553B Subsystem.

The user custom logic is installed on FPGA after installing CPU IP Core and Core1553BRT_APB. The implemented user custom logic is linked with Core1553BRT_APB block. The FABRIC_APB3 user custom logic is extended to connect to the APB bus and allow expand to command legality judgment.

Finally, we connected all of the installed modules. The routing scheme for functional block is shown in Fig. 4 in detail.

Transceiver and transformer of the MIL-STD-1553B are connected to external circuit because controller IP Core of the MIL-STD-1553 does not include bus transceiver and transformer.

III. Performance Evaluation

For verifying a performance of the MIL-STD-1553B system based on the proposed system, simulation environments are constructed with implemented devices. The simulation environment is shown in Fig. 5.

After the Core1553BRT_APB IP receives a message which generates an interrupt, decodes the command word of the message and processes the next operation of the RT. The Core1553BRT_APB is used to store received data word or transmit the data word to the MIL-STD-1553B data bus.

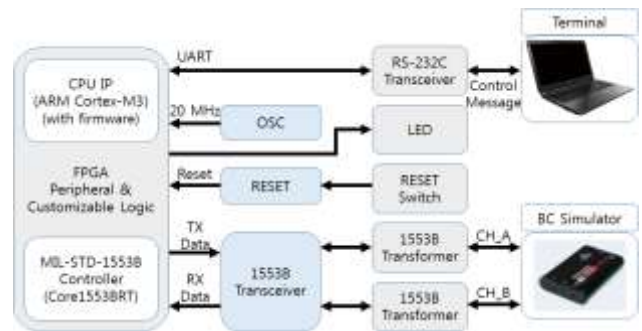


Figure 5. FPGA based Subsystem Control Module.

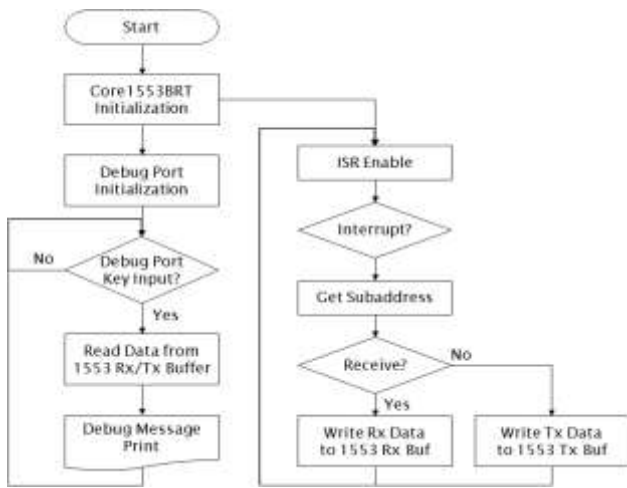


Figure 6. Flowchar of Implemented Firmware.

The data to be transmitted is handled by the firmware of the processor which connect with Core1553BRT_APB and APB. The flowchart of implemented firmware in this research is shown in Fig. 6. Firmware is able to inquire control register of IP Core and it is implemented to transmit and receive data in real time.

The functional test items were selected from the MIL-STD-1553 standard that can be measured and implemented in the test bench. The electrical characteristics of the MIL-STD-1553B RT system module were tested by sample messages. The sample message was generated by MuxSim software to generate RT to BC and BC to RT messages in one frame. After transmitting the frame, the signal differential of the MIL-STD-1553 transformer was measured with an oscilloscope.

The reception level of the command word which is specified by the MIL-STD-1553B standard is 1.0 to 20.0 Vp-p. As a result of simulation, it meets the criterion at 12.0 Vp-p as shown in Fig. 7. The specified status word output level is 18.0 to 27.0 Vp-p. As a result of simulation, it meets the criterion at about 20.6 Vp-p as shown in Fig. 8. The response time specification is under 4.0 μ s. The response time for the BC command word is 3.7 μ s as shown in Fig. 9. The message interval specification is more than 4.0 μ s and the interval between the two sample messages meets the criterion as 7.4 μ s as shown in Fig. 10.

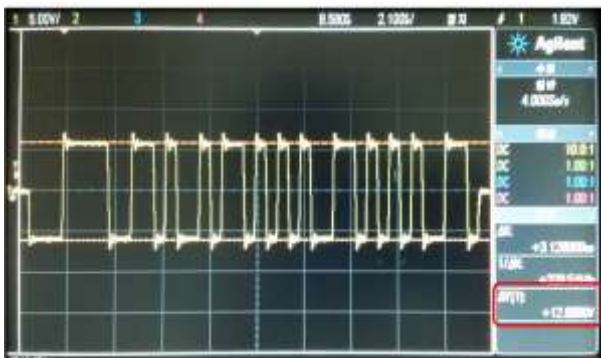


Figure 7. Measurement of Receive Level of RT Command Word.

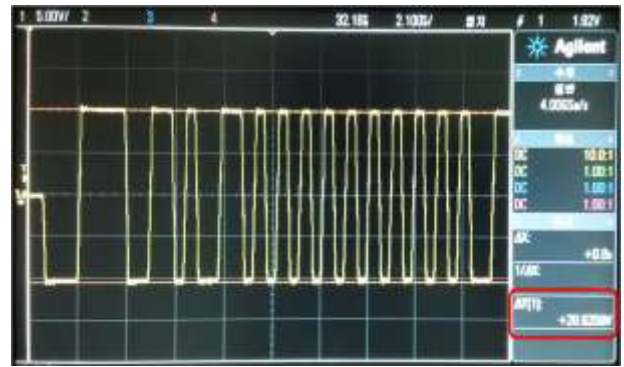


Figure 8. RT Status Word Output Level.

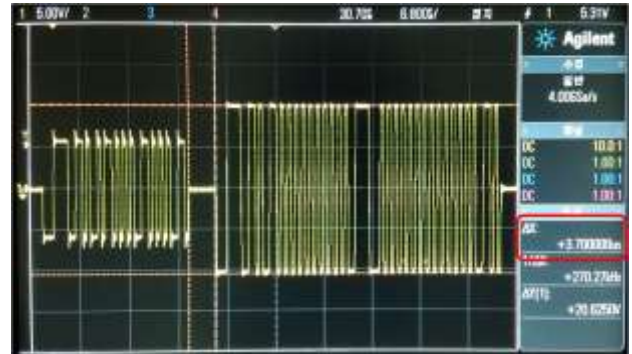


Figure 9. RT Response Time Measurements.

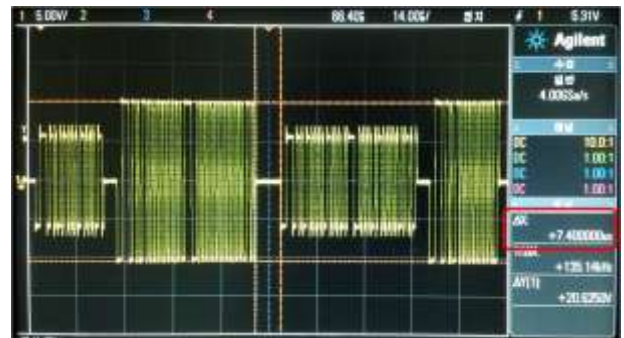


Figure 10. Measurements of Message Gap.

iv. Conclusion and Future Works

In this paper, we propose design and implementation FPGA based RT subsystem of the MIL-STD-1553B for military system requiring high reliability.

The prototype of the RT subsystem was implemented based on the design method. The one-to-one data communication with BC and the communication function between RTs were tested and analyzed using prototype of RT subsystem. In simulation results, following advantages were obtained.

First, all the components which is needed to operate as RT subsystem except the MIL-STD-1553 transceiver and transformer can be combined into a single FPGA device. The number of components is reduced and the degree of integration is increased because of this. Second, by replacing the MIL-STD-1553 controller ASIC and CPU with IP Core,

technology reliance was reduced and manufacturing costs were reduced due to the reusable IP Core feature. Third, the proposed technique is easy to maintain because both hardware and software functions are programmable.

In future work, we will study the module design method of the dual MIL-STD-1553B bus to provide multi-function and multi-channel operation in one module.

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