

Lumped RF Model of MOSFET Gate Resistance for GHz+ Frequencies

Enhancement of Compact BSIM MOSFET Model

[Stanislav Banáš, Charles Hoggatt, Václav Paňko, Josef Dobeš, Jan Divín]

Abstract— This paper presents a lumped RF model of high voltage FET applicable for the frequency up to GHz range. Unlike the compact MOSFET model, the proposed solution contains not only parasitic capacitances and resistances but also parasitic inductance. The signal delay caused by relatively large device area including the parasitic resonance modeled by distributed RLC network is considered. The model is applicable in commercial SPICE simulators, e.g. Eldo, Spectre or HSpice.

Keywords—SPICE model, MOSFET, RF, parasitic, RLC network, high frequency, GHz, simulation

I. Introduction

Nowadays the design of competitive integrated circuits requires short cycle time and first pass success in manufacturing. This is assured by precise SPICE models. The commercial simulators contain many compact models, e.g. BSIM [1], PSP [2] or HISIM [3] for MOSFETs, Gummel-Poon [4] or VBIC for bipolar transistors, containing set of tunable parameters. However, the high voltage and high frequency area is not yet fully covered by compact models. Therefore the macro-models built from the combination of compact model with the parasitic RLC network or behavioral HDL blocks must be created.

This paper is focused on the modeling of fast high voltage MOSFET used as an output stage, operating in frequencies in order of GHz and voltages up to $V_{ds}=30V$ and $V_{gs}=8V$. Due to very large gate width ($w_g \sim 3m$) the MOSFET has very low on state resistance R_{dson} and due to the construction it has very low output capacitance. The typical R_{dson} is in order of miliohms, gate-drain capacitance is in order of picofarads and gate source capacitance in order of nanofarads. Although the total gate width is very large, in order of meters, the device total area is relatively small, in order of square millimeters, due to the high integration (see layout in Figure 1 and Figure 2).

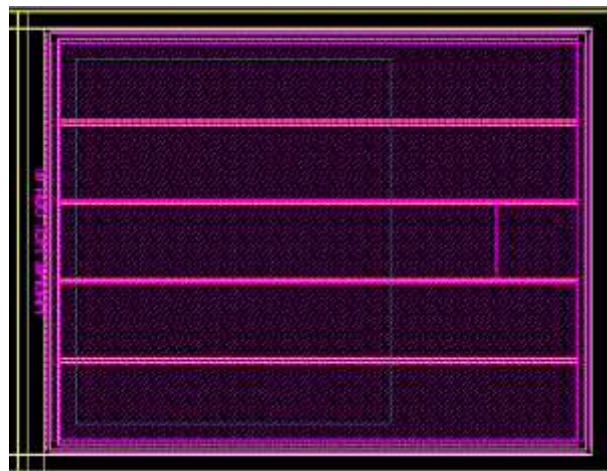


Figure 1. Layout of characterized high voltage MOSFET with area $\sim 3mm^2$

Such a device of course contains many parasitic phenomena not observed in standard MOSFETs. Namely the gate impedance including the imaginary part has to be considered. Especially the inductance part because the density of gate connections is in our case quite large as demonstrated in Figure 2.

The compact BSIM4 model was used for the modeling of basic MOSFET. Although this model contains gate resistance parameters, the measured data were too different from the expected characteristics. So it was decided to use RLC network instead.

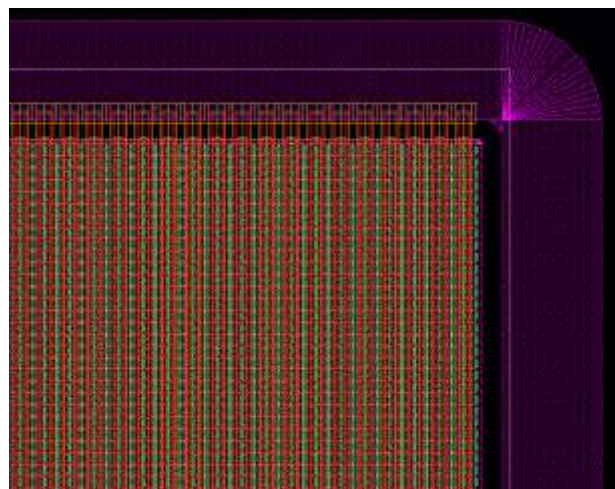


Figure 2. Layout of characterized high voltage MOSFET – detail $\sim 50 \times 50 \mu m$

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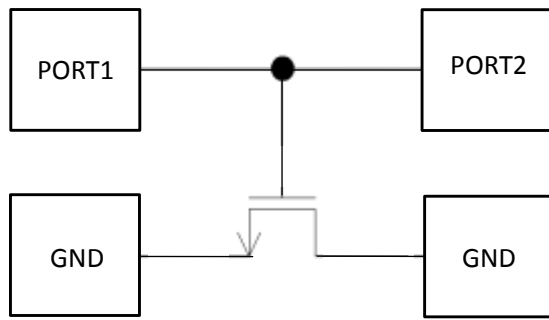


Figure 3. Ground-Signal two-port structure for S-parameters measurement

II. Model development

The scalable model was created based on the standard SPICE modeling methodology [5,6,7]. The test-mask containing required device in several configurations, namely various gate width, number of rows, and number of columns was designed. The device was measured in full operation area up to maximal voltages and in full temperature range (-40...+150°C). The test plan contained DC methods (IdVd, IdVg), capacitance methods (Cgd, Cgs), and Transmission Line Pulse (TLP) tests for the measurement of high currents to prevent self-heating. The measured data were then used for the extraction of BSIM4 MOSFET model parameters.

Finally, the frequency measurement of S-parameters using Ground-Signal structure demonstrated in Figure 3 and network analyzer Agilent 8753 operating up to frequency 2GHz was performed. As it can be seen in Figure 3, the MOSFET has grounded drain and source, so the measured Z_{12} impedance corresponds to the MOSFET in series with gate resistance. The measured S-parameters were transformed to Z parameters using standard transfer functions.

The most of compact MOSFET models contain only parasitic capacitance and do not calculate with parasitic gate impedance. The measured DUT can be then simplified to the gate resistance in series with the parallel combination of gate-drain and gate source capacitances. Such a model is very

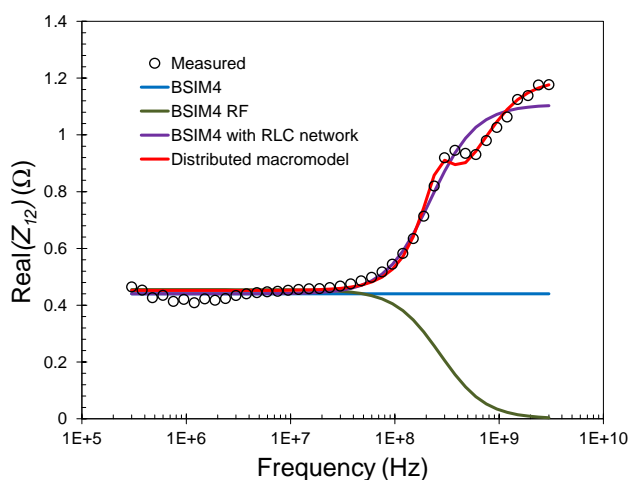


Figure 4. Real part of Z_{12} impedance, comparison of simulated results with measured data

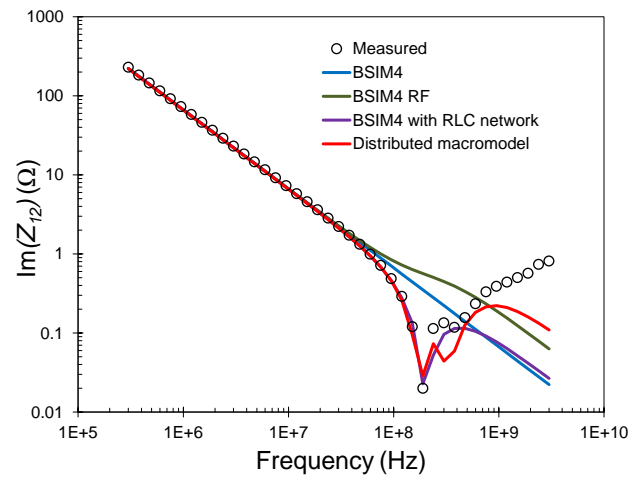


Figure 5. Imaginary part of Z_{12} impedance, comparison of simulated results with measured data

simple and the Z_{12} impedance can be expressed by the simple equation

$$Z = R + \frac{1}{j\omega C} \quad (1)$$

where R corresponds to gate resistance and C corresponds to parallel combination of gate-drain and gate-source capacitances. Bulk is here shorted to the source, so the gate-bulk capacitance is here considered as a part of gate source capacitance. However, such a model was in our case insufficient, as demonstrated in Figures 4-7. Blue line represents the simulation with the standard compact MOSFET BSIM4 model, circles represent measured data.

The BSIM4 MOSFET model contains set of RF parameters for the gate resistance modeling [1] but they represent just parallel combination of gate resistance and capacitance. This is sufficient for standard CMOS but not for our power device with strong influence of parasitic inductance. Therefore the implementation of BSIM4 RF model made simulation results even worse, as it is depicted in Figures 4-7, green line.

Therefore it was decided to use the external RLC network demonstrated in Figure 8. Except gate-drain and gate-source capacitors which are part of the compact BSIM4

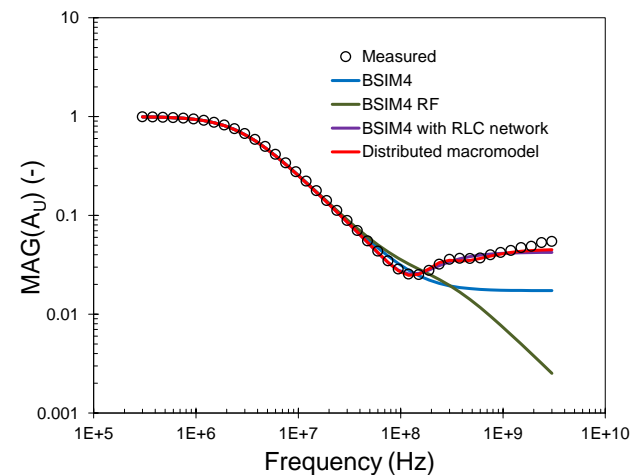


Figure 6. Magnitude of transfer function, comparison of simulated results with measured data

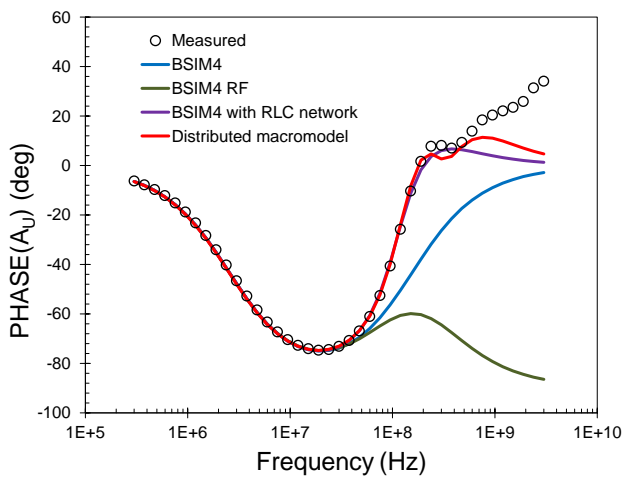


Figure 7. Phase of transfer function, comparison of simulated results with measured data

model, all other components are modeled by separate resistor and inductor compact models. The parameters of external RLC networks were extracted from several dimensions of MOSFETs measured in Ground-Signal structure demonstrated in Figure 3. The simulated results are demonstrated in Figures 4-7, purple line.

Although the agreement with measured results is in this case much more promising than in previous two cases, there are still discrepancies. Especially in frequency range of MHz the strong non-idealities visible mainly in real part of impedance can be observed. Peaks in about 200MHz are probably caused by the resonance of RLC network created by high density of gate connectors that behave in high frequencies like inductors.

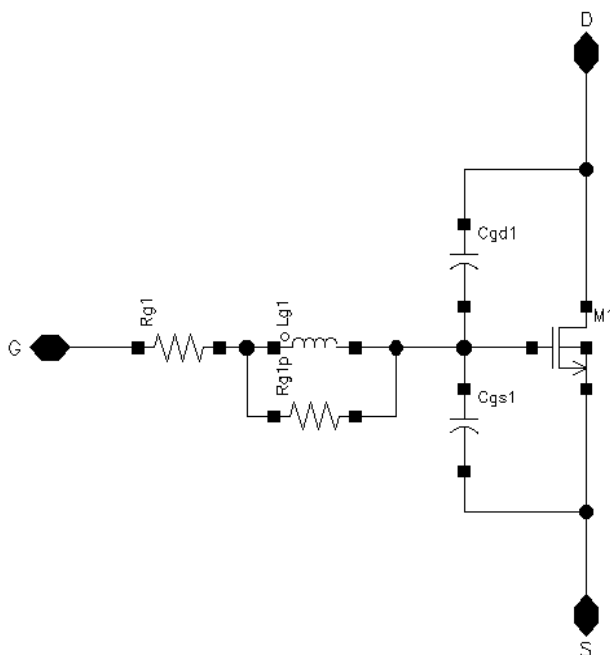


Figure 8. Macromodel – first prototype

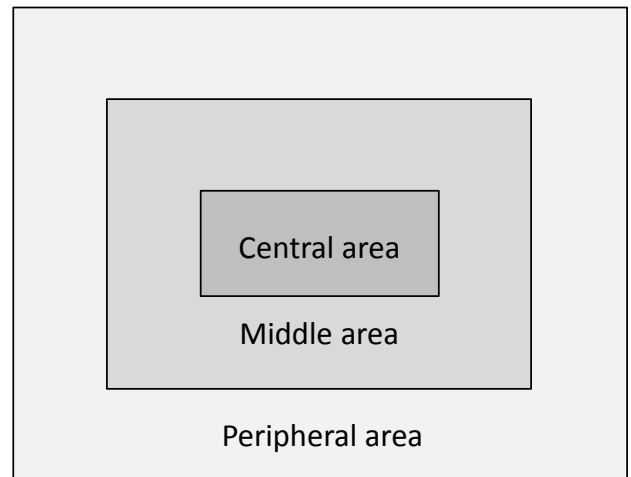


Figure 9. MOSFET Layout segmentation for the modeling of signal delay

III. Final Results

It was discussed that for the precise modeling of such complex characteristics the large device area and the signal delay should be considered. The signal comes faster to the periphery parts of the device than to the central parts which should be considered by the model. The idea of the model is demonstrated in Figure 9: to split the device to three parts, central area, middle area and peripheral area, where the signal comes to the central area longer than to the peripheral area. The RLC network representing the gate signal path to the central area must contain larger R, L and C values than the RLC network representing the gate signal path to the peripheral area. The final macro-model created by three parallel MOSFETs where each represents one third of gate width is depicted in Figure 10. Three RLC networks are then connected such a way, that the signal coming to the MOSFET representing central area goes through three RLC networks, the signal coming to the MOSFET representing the middle area goes through two RLC networks, and finally the signal coming to the MOSFET representing peripheral area goes through one RLC network. This distribution assures more realistic signal delay. And finally, the right extraction of RLC values of these three segments covers above mentioned resonance effect in MHz range.

The various dimensions of the device were used for the RLC network parameter extraction to cover the scalability of the device, especially the dependency on the input parameters, which are gate width of the segment, number of segments in line, number of segments in columns – see Figure 2. Moreover, the dependency on the gate pad position and editable width of metal gate was implemented. Final model vs data plots are demonstrated in Figures 4-7, red line vs circle data points. The agreement with measured data is in this case very good.

IV. Conclusion

The enhanced accurate RF model of high voltage power MOSFET for GHz frequency range has been created and presented in this paper. The modeling results were compared with measured data and with other concepts of models. The

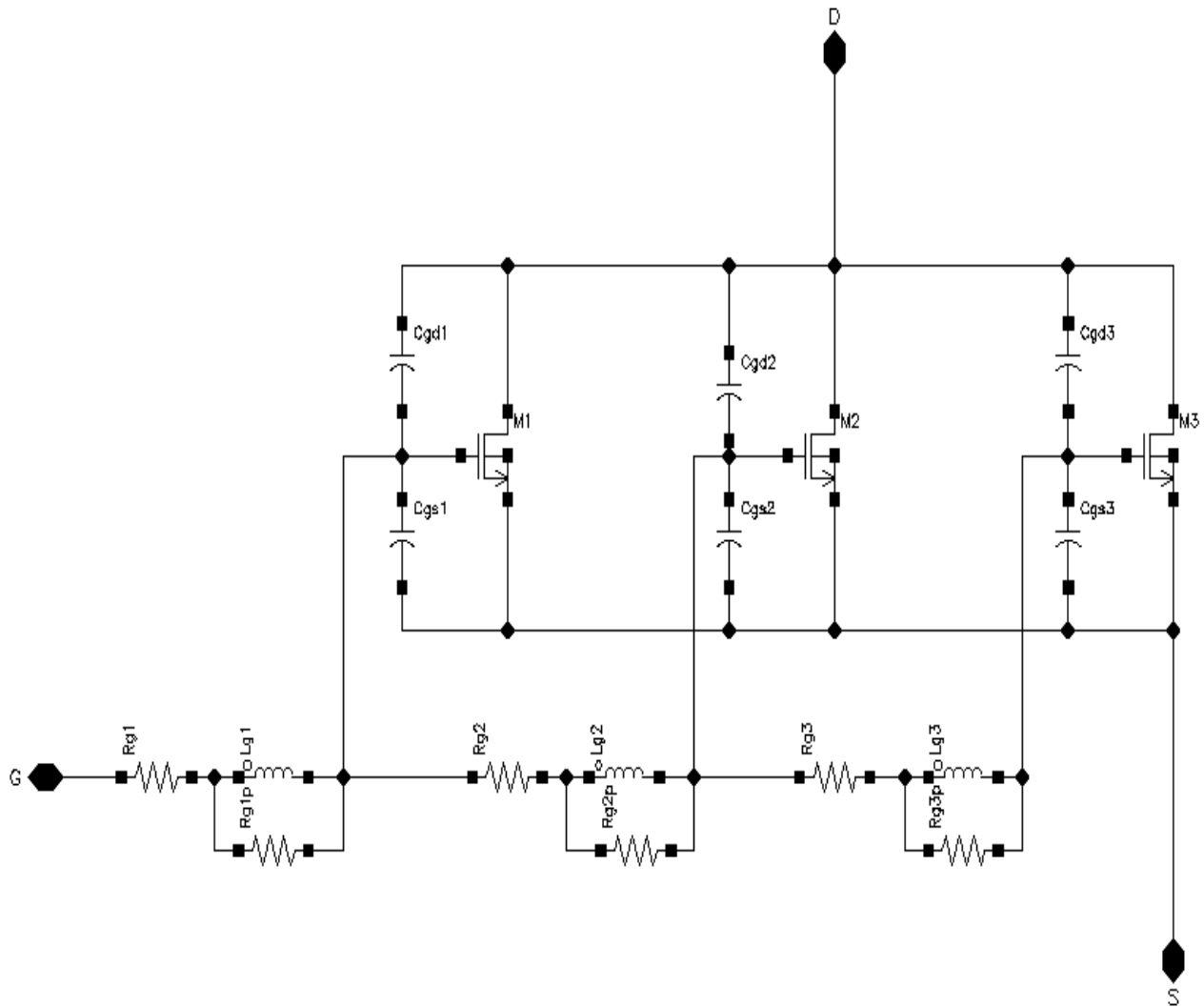


Figure 10. Macromodel – final solution

model was validated in full temperature range and operation range. It's fully scalable and valid even for very large dimensions. It was proved that the model has smooth derivatives of all simulated characteristics and therefore has very good convergence and simulation speed. The model can be used in standard commercial simulators which was verified in Eldo, Spectre and Hspice.


v. Acknowledgements


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