Performance Comparison of Oscillator Circuit Topology for MEMS SAW Resonator

Jamilah Karim , Anis Nurashikin Nordin, Rafidah Rosman

Abstract— **This paper presents the simulation results and the performance comparison for three different pierce oscillator circuit topologies. The oscillators were based on the CMOS MEMS SAW resonator. The designs were simulated using 0.35um CMOS technology. Design_3 has the best phase noise performance and settling time as compared to the other two topologies namely Design_1 and Design_2. The settling time for Design_3 was 10ns and the phase noise performance was -90.3dBc/Hz at 10-kHz offset frequency. Design_2 required 40ns to achieve stability where the phase noise performance was -80.1dBc/Hz at 10-kHz offset frequency. Meanwhile, Design_1 required 30ns before it could achieve stability and the phase noise performance was -56.8dBc/Hz at 100-kHz offset frequency. Phase noise performance was the most important criteria for oscillator where in most cases, the resonator used in an oscillator must have high Q in order for the oscillator to have good phase noise performance. However, the sustaining amplifier circuit could also be used to improve the phase noise performance of the oscillator**.

Index Terms—**MEMS based Oscillator, MEMS resonator, MEMS SAW resonator, Pierce Oscillator**

I. INTRODUCTION

Oscillators are crucial building blocks in transceiver and most electronic platforms. Wireless communication circuits rely on oscillators as stable frequency references to facilitate system synchronization, signal modulation and timing [1].Quartz crystal resonators have traditionally been the most popular form of clock generators. Yet quartz crystals cannot be integrated with microelectronics, losing their high Q advantage to lossy bond wires and large form factors. The motivation for integrated frequency references include smaller form-factors, lower cost, greater flexibilities, higher reliability and batch processing. Efforts to replace quartz technology with more 'silicon-friendly' technologies include CMOS oscillators and silicon micro-electro-mechanical-systems (MEMS) oscillators. CMOS oscillators or electrical oscillators

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rely on LC filters to select their frequencies and are defined by their low-Q CMOS inductors. This ranges from 10-20 [2]. In contrast, MEMS oscillators utilize mechanical vibrations as their frequency selective element and exhibit Qs in the order of millions [3]. Silicon-compatible MEMS resonators can be fabricated on a CMOS [4] or packaged with CMOS circuits in a single package [3]. Silicon-compatible MEMS resonators were preferred due to their reduced size, cost and increased level of system integration.

This work illustrates different oscillator topologies which are suitable for a CMOS MEMS SAW resonator. Basic oscillator topologies are discussed in Section II while Section III explains the oscillator circuit design. The simulation output and discussion is explained in Section IV and Section V concludes the paper.
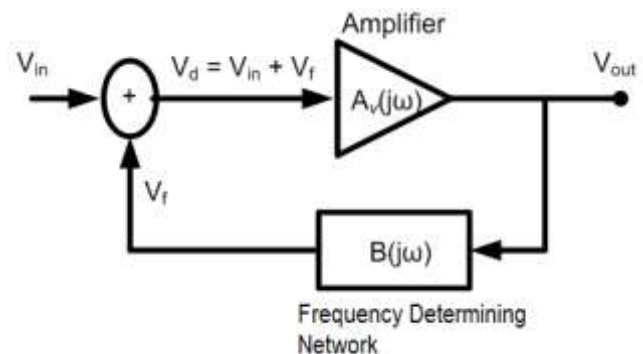
II. OSCILLATOR TOPOLOGIES

Figure 1: Basic Oscillator System

The basic oscillator system which comprises of an amplifier circuit and its frequency determining network is shown in Figure 1. The frequency determining network can either be the resonator or the RC or LC circuit. In this work, the frequency determining device used was a MEMS SAW resonator.

CMOS MEMS SAW resonator is made from piezoelectric material. This resonator was introduced in [5] . The resonance frequencies of CMOS MEMS SAW resonator ranges from 600MHz to 3.12GHz while the Q factor ranges from 33 to 94[5]. The resonators were formed when the two IDTs were placed between the reflectors. Reflectors are key components of the SAW resonator. The reflectors will restrain the outward propagating wave within the cavity and thus reduces the losses. Here, the IDT_1 is the transmitter while IDT_2 is the receiver. From Figure 2, IDT_1 is connected to V_{in} and IDT_2 is short circuit to sense the current I_{out}. The operating principle of SAW device is based on the piezoelectric effect. When a

microwave voltage input was applied at the transmitting (input) IDT, it generates a propagating acoustic wave on the surface of the substrate. This propagating acoustic wave in turn produces an electric field localized at the surface which can be detected and translated back into an electrical signal at the output IDT port. Thus, with the existence of reflector, the resonance frequency can be created.
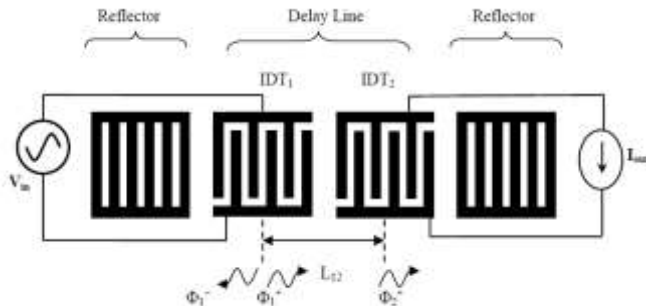

Figure 2: Schematic of two-port SAW resonator

Since MEMS SAW resonators are lossy, they typically require amplifiers to start and sustain oscillation. The sustaining amplifier circuits define the oscillator topology where there are several oscillator topologies namely; pierce oscillator, transimpedance amplifier, differential amplifier, colpitts oscillator, Hartley oscillator and cross coupled oscillator. However, MEMS based oscillator used only differential amplifier circuit[6], pierce circuit[7]–[11] and transimpedance amplifier circuit[12]–[16]. The topology chosen is normally based on the design specifications such as low power and low noise oscillator. Besides that, the R_x and the insertion losses of the resonator contribute to the suitability of the topology chosen.

Table 1:
DC PERFORMANCE OF THE OSCILLATOR CIRCUIT TOPOLOGIES

Ref.	Amplifier Topology	DC Performance
[7]	Pierce Circuit	$g_m = 10.47mS$ $V_{ds} = 764mV$ $I_d = 582.4\mu A$
[17]	Pierce Circuit	$g_m = 12.6mS$ $V_{ds} = 731mV$ $I_d = 554.1\mu A$
[9]	Pierce Circuit	$g_m = 8.33mS$ $V_{ds} = 736mV$ $I_d = 535.8\mu A$
[10]	Pierce Circuit	$g_m = 2.55mS$ $V_{ds} = 812mV$ $I_d = 669\mu A$
[18]	Transimpedance Amplifier Circuit	$g_m = 3.16mS$ $V_{ds} = 1.09V$ $I_d = 535\mu A$
[19]	Transimpedance Amplifier Circuit	$g_m = 2.56mS$ $V_{ds} = 795.2mV$ $I_d = 638.8\mu A$
[16]	Transimpedance Amplifier Circuit	$g_m = 2.73mS$ $V_{ds} = 765.2mV$ $I_d = 598.8\mu A$

Among all the topologies mentioned, pierce circuit is the simplest, provide straightforward biasing and easier to design.

Pierce circuit topology and TIA circuit topologies in [7]–[10], [14]–[16] was simulated using MIMOS 0.35µm technology. Their DC simulation results are summarized in Table 1. Clearly, the result in Table 1 shows that pierce circuit topologies result in very high transconductance, g_m compared to TIA circuit topologies. The g_m of Pierce circuit topologies ranges from 2.55mS to 12.6mS. The topology introduced by [8] yielded the highest g_m which was 12.6mS at $V_{ds}= 731mV$ and $I_d= 554.1\mu A$. Meanwhile, the Pierce topology introduced in [10] only produced $g_m = 2.55mS$. This topology was biased with $V_{ds}= 812mV$ and $I_d= 669\mu A$. Both circuits were based on inverter circuit, but the Pierce circuit in [8] has the feedback impedance that provided sufficient impedance to ensure the necessary g_m was achieved. The TIA circuit topologies shown in this table produced g_m from 2.56mS to 3.16mS. The topologies biased at V_{ds} from 765mV to 1.09V. The bias current for the lowest g_m for TIA circuit topology was 638.8µA while the highest g_m was 535µA.

Both topologies did not show much difference in terms of their biasing of V_{ds} and I_d. However, with slight differences Pierce circuit topology yielded very high g_m. Therefore, Pierce circuit topologies are highly recommended to be used in oscillator circuit design for this work.

III. PIERCE OSCILLATOR CIRCUIT DESIGN

The oscillator generated oscillation without any external input. The sustaining circuit or the amplifier circuit with the ability of self-sustaining allowed its own noise to grow and developed the periodic signal. The performance of the MEMS base oscillator is not only dependent on the resonator but also on the supporting circuit.

To provide the oscillation, the MEMS resonator will normally be embedded in the feedback loop of an amplifier as shown in Figure 1. To achieve oscillation, the Barkhausen criterion was necessary but not sufficient [20]. To ensure oscillation in the presence of temperature and process variation the loop gain has to be chosen at least twice or three times the required value [21]. The criterion is written in equations (3) and (4) below.$|\beta(j\omega)A_v(j\omega)| = 1$ (1

$$|\beta(j\omega)A_v(j\omega)| = 1 \tag{1}$$

And

$$\angle\beta(j\omega)A_v(j\omega) = \pm n360° \tag{2}$$

where n=0,1,2,3……………………

Pierce oscillator circuit topology was chosen in this work. The choice of the topology was based on the need for low power consumption and low phase noise. This topology was often chosen for its low frequency quartz crystal oscillators (Otis, 2002). Pierce circuit topologies were well known for its frequency stability and can be used for a wide range of frequencies. Besides the circuit simplicity it has, the topology was also ideal for low current and low voltage circuit design (Otis, 2002) as they provided straight forward biasing.

Three Pierce Oscillator circuits topology were used to analyze the performance of CMOS oscillator based on CMOS MEMS SAW resonator, R3_S2. Figure 3 and Figure 4 show the detail schematic diagram of Pierce Oscillator circuit topology integrated with the resonator R3_S2 respectively. In later parts of the discussion, the topology in Figure 3 is called Design_1 while the topology in Figure 4 is called Design_2. The results were then being compared with the performance of Pierce oscillator circuit of Figure 5 known as Design_3. All the three topologies in Figure 3, Figure 4 and Figure 5 showed that the pierce oscillator will amplify the signal from the resonator output and fed the signal back to the resonator. Thus, the oscillation was sustained.

T_1, T_4 and T_7, are the single stage pierce circuit topology for Figure 3 and Figure 5, while for Figure 4 where the first stage consist of T_1, T_4, T_5 and T_9. T_1 is the main transistor that provides the critical transconductance for oscillation and was biased by transistor T_4. Besides providing the bias resistance to the gate of T_1, T_7 and T_9 also provided enough resistance to ensure that the oscillation could be sustained. The rest of the transistors in the figures were then added to become the second and third stages in order to ensure that the oscillation could be started and sustained.
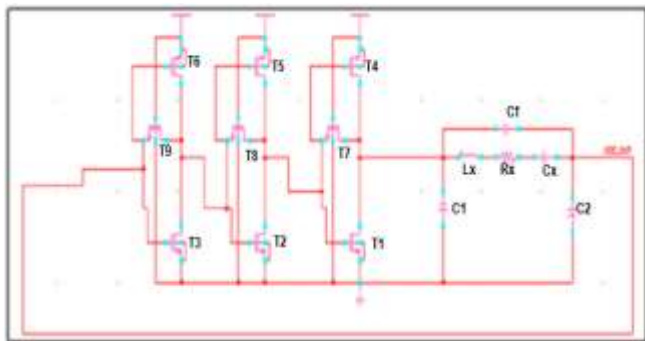

Figure 3: Detail schematic of Pierce Oscillator circuit topology for Design_1
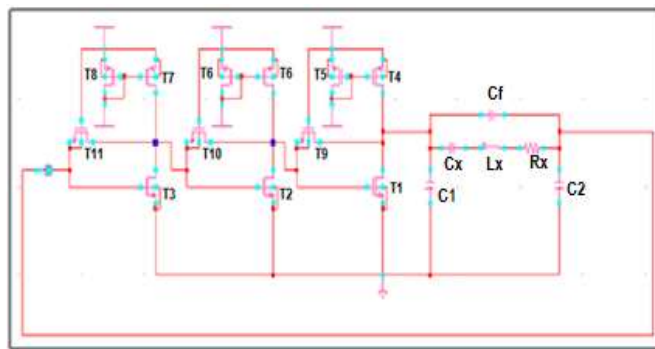

Figure 4: Detail schematic of Pierce Oscillator circuit topology for Design_2
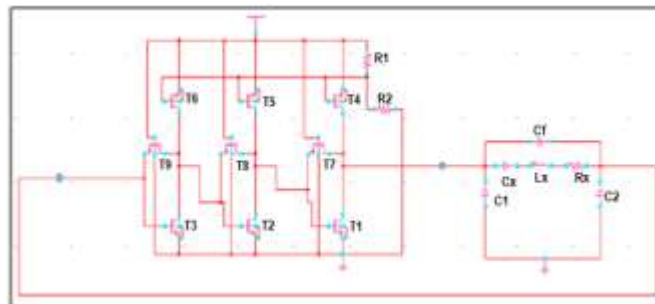

Figure 5: Detail schematic of Pierce Oscillator circuit topology for Design_3

The equivalent circuit parameter of MEMS SAW resonator used in this work is summarized in Table 2.

Table 2:
PARAMETER OF MEMS SAW RESONATOR

Element	$R_x(\Omega)$	$L_x(uH)$	$C_x(fF)$	C_f (fF)	$C_1=C_2$ (fF)
R3_S2	185	1.6	5	143.8	300

Table 3 shows the DC operating parameters for all the 3 oscillator topologies during oscillation. Design_2 was biased at 0.921mA while Design_1 and Design_3 was biased at 1.1mA. The biasing voltage for Design_1, Design_2 and Design_3 were 0.72V, 0.811V and 0.750V respectively. The power consumed by all the designs when integrated with R3_S2 is 2.38mW for Design_1, 2.24mW for Design_2 and 2.47mW for Design_3. The highest power consumption is topology in Design_3 and the lowest power consumption is topology in Design_2. It is then clear that the oscillator to be used in wireless systems should consume a minimum amount of power. However, since the SAW resonator used in this work has large values of C_1 and C_2, larger bias current was then required. Therefore, larger power was required to sustain the oscillation for this oscillator based on the MEMS SAW resonator.

Table 3:
DC operating parameters at which the oscillators oscillate

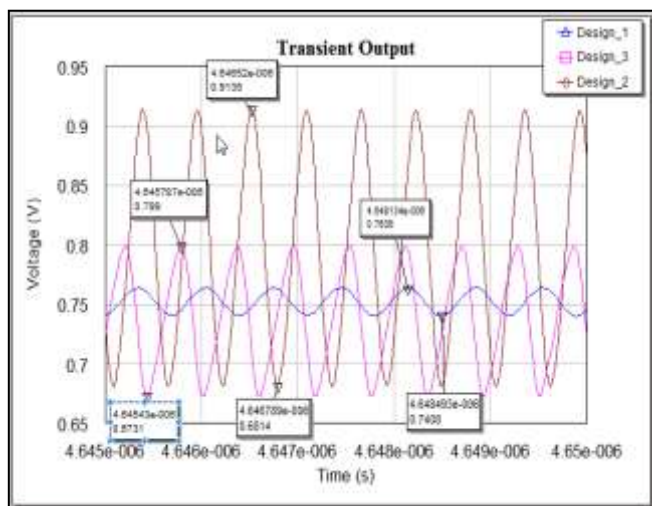| Element	V_{dd} (V)	I_d (mA)	V_{ds} (V)	g_m (mS)	$P_{consume}$ (mW)
Design_1	3	1.100	0.720	10.6	2.38
Design_2	3	0.921	0.811	6.6	2.24
Design_3	3	1.100	0.750	9.6	2.47

Figure 6: Transient Output for three different topologies simulated with R3_S2

The transient output of all the three Pierce topologies was plotted in Figure 6. Design_2 shows the highest amplitude oscillation which was 232mV and generating a 1.77GHz frequency. The amplitude oscillation for Design_3 is 126mV at 1.75GHz resonance frequency. While Design_1 yielded very low voltage output among the three which was 23mV with achievable resonance frequency at 1.5GHz. This was far from the resonance frequency of the MEMS SAW resonator.
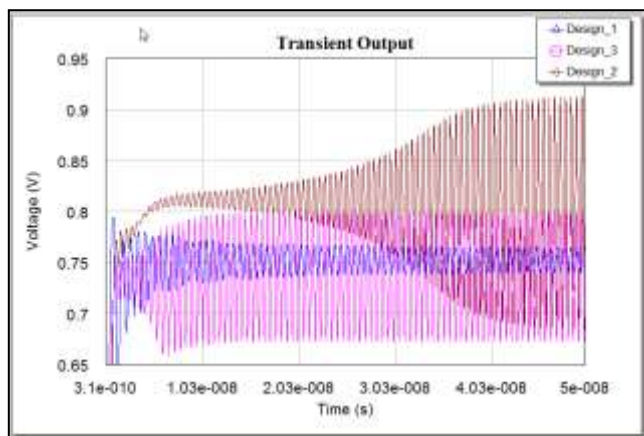

Figure 7: Settling time for three different topologies simulated with R3_S2

Figure 7 shows the settling time for the three topologies when simulated with resonator R3_S2. The figure clearly show that Design_2 required 40ns to achieve stability while Design_1 required 30ns. Apparently, Design_3 has the shortest settling time which was only 10ns. The settling time will determine how fast the systems respond from one frequency to another.
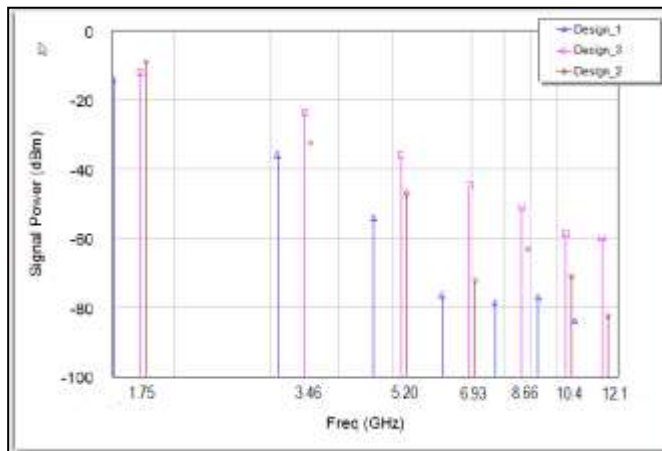

Figure 8: Power Spectrum for three differ rent topologies simulated with R3_S2

Spectrum signal for all the three topologies are shown in Figure 8. The spectrum for topology in Design_2 is -9dBm at 1.78GHz resonance frequency. Design_1 topology resulted in lowest spectrum when integrated with R3_S2, which was -17dBm at 1.55GHz resonance frequency. Meanwhile, Design_3 topology resulted in -14.5dBm spectrum signal at 1.75GHz resonance frequency.
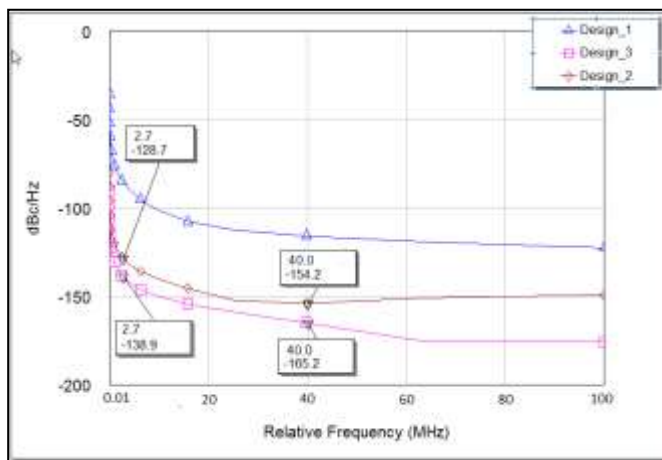

Figure 9: Phase Noise Performance for three different topologies simulated with R3_S2

Figure 9 shows the phase noise performance for three different Pierce oscillator circuit topologies. As shown in the figure, the simulated phase noise of the output signal from Design_1 topology was −56.8dBc/Hz at 100-kHz offset frequency with a floor of −120dBc/Hz. The phase noise of Design_2 and Design_3 were −80.1 dBc/Hz and -90.3 at 10-kHz offset frequency respectively and the noise floor for Design_2 was −150.4 dBc/Hz and for Design_3 at -

175.6dBc/Hz. The phase noise performance of Design_2 and Design_3 topology was better than design_1. Obviously, Design_3 has the best phase noise performance and the lowest noise floor when compared with the other two oscillators' topologies. The Leeson phase noise equation is expressed in equation 5 below.

$$\mathcal{L}_{fm} = 10log\left[\frac{FkT}{P_{sig}}\frac{1}{8Q_L^2}\left(\frac{f_o}{fm}\right)^2\right] \qquad (5)$$

Where L_{fm} is the single side band Phase Noise, P_{sig} is the oscillator output power, F is the active device noise factor, k is the Boltzmann's constant, T is the temperature, f_o is the oscillator resonance frequency, f_m is the offset frequency and Q_L is the loaded Q. Loaded Q exist when a resonator was connected to the sustaining circuit, their total losses were combined. Thus, although Design_2 has higher signal spectrum as compared to Design_3, extra CMOS in the sustaining circuit will overload the overall circuit and degraded the performance.

V. CONCLUSION

The simulation and the comparison of CMOS oscillators based on CMOS MEMS SAW resonator has been discussed in this paper. The oscillators have been simulated using three different Pierce oscillator circuit topologies. The result showed that topology from Design_3 has the best phase noise performance and settling time as compare to the other two topologies in Design_1 and Design_2. The settling time for Design_3 is 10ns and the phase noise performance was -90.3dBc/Hz at 10-kHz offset frequency. Design_2 required 40ns to achieve stability and the phase noise performance was -80.1dBc/Hz at 10-kHz offset frequency. Meanwhile, Design_1 required 30ns before it can achieve stability and the phase noise performance was -56.8dBc/Hz at 100-kHz offset frequency. Phase noise performance is the most important criteria for oscillator. In most cases, the resonator used in an oscillator must have high Q in order for the oscillator to have good phase noise performance. However, the sustaining amplifier circuit can also be used to improve the phase noise performance of the oscillator. Thus, the discussion of the future oscillator design for CMOS MEMS SAW resonator will be based on pierce topology in Design_3.

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