Design of FIR filter using Kaiser Window

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Abstract:The Finite Impulse Response (FIR) filter is a digital filter widely used in Digital Signal Processing applications in various fields like imaging, instrumentation, communications, etc. Programmable digital processors signal (PDSPs) can be used in implementing the FIR filter. However, in realizing a large-order filter many complex computations are needed which affects the performance of the common digital signal processors in terms of speed, cost, flexibility, etc. By using Kaiser window attempt is made to reduce the sidelobe level & control by modifying nth order Bessel function $I_0(x)$& controlling the shape factor by adjustable parameter α. Few dB sidelobe level response is also reduced. In this paper the design of digital FIR filter has been discussed.

Keywords: FIR filter, digital filters, FPGA, Kaiser Window, passband, stopband

INTRODUCTION

Earlier work in this direction has been carried out **V. Soni, P. Shukla and M. Kumar (2011)** & proposed that the Exponential window provides better side-lobe roll-off ratio than Kaiser window which is very useful for some applications such as beam forming, filter design, and speech processing. Besides this a design of digital nonrecursive Finite Impulse Response (FIR) filter by using Exponential window was proposed. The far-end stopband attenuation is most significant parameter when the signal to be filtered has great concentration of spectral energy.

Z. Yu, M.L. Yu, K. Azade and A. N. Willson (2010) tried to exploit the sign-extension property of a 2's complement number and proposed a reduced representation of 2's complement numbers to avoid sign-extension. Instead of having the high switching activity at the MSB side of the data path, the proposed number representation avoids switching of the MSBs altogether, and therefore reduces the power dissipation in digital arithmetic circuits.

R. A. Kennedy Abhayapala introduced a novel sinhc kernel which generates a Kaiser window based TFD. Time-frequency distributions (TFDs) have been used as a tool to locate the time dependency of the spectrum in analysing non-stationary signals. The Kaiser window has been used extensively in designing finite impulse response digital filters, and in other digital signal processing applications. The Kaiser window is an asymptotic approximation to the prolate spheroidal wave functions, which have been shown to provide concentration of energy simultaneously in time and frequency and thus showed that Kaiser distribution is a member of the Cohen class, and the corresponding kernel satisfies all the desirable kernel properties. Besides this they showed that the shape of the Kaiser window can be used to control the trade-off between auto-term and cross-term energy.

N. H. Phuong discussed FIR Filter Design with the Window Design method. The design of a FIR filter starts with its specifications in either discrete-time domain or DTFT frequency domain, or both. In the time domain, the design objective is the impulse response. In the frequency domain, the requirement is on various parameters of the magnitude response. Analyzing all the fixed windows, the only adjustable length $(M+1)$ was of Kaiser window. The Kaiser window has an additional ripple parameter β, enabling the designer to trade off the transition and ripple.

CONCEPT OF FILTR DESIGN

The fundamental concept of FIR filter design is that the filter frequency response is determined by the impulse response & quantized impulse response & the filter coefficients are identical. The input to FIR filter is an impulse, and as the impulse propagates through the delay elements, the filter output is identical to the filter coefficients. The FIR filter design process therefore consists of determining the impulse response & then quantizing the impulse response to generate the filter coefficients. The design of a digital filter involves five steps - Filter specification ii) Filter coefficient calculation, iii) Realization, iv) Analysis of finite word length effects and v) Implementation This involves producing the software code and/or hardware and performing the actual filtering. These five inter related steps are summarized by flow chart:
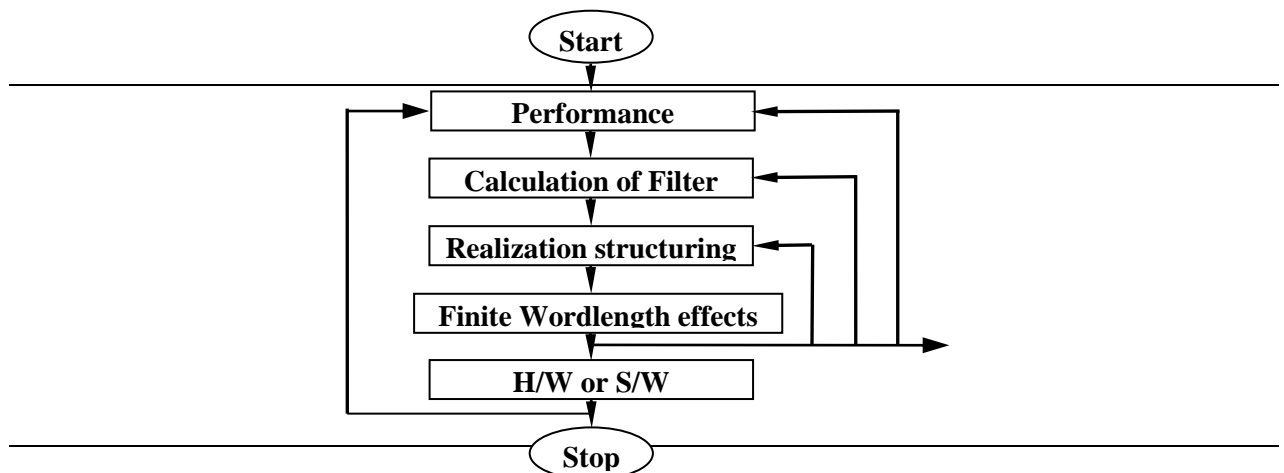
In the passband, the magnitude response has a peak deviation of δ_p and in the stopband, it as a maximum deviation of δ_s. The width of transition band determines how sharp the filter is. The magnitude response decreases monotonically from the passband to stopband in this region.

The following are the key parameters of interest:

δ_p peak passband deviation (or ripples)

δ_s stopband deviation.

f stopband edge frequency.

f_p passband edge frequency.

f_s sampling frequency.

The edge frequencies are often given n the normalized form, that is as the fraction of the sampling frequency (f/F_s). Passband and stopband deviation may be expressed in decibels. When they specify the passband ripples and minimum stopband attenuation respectively.

Thus the minimum stopband attenuation, A_s and the peak passband ripple, A_p, in decibels are given as:

$$A_s \quad \text{(stopband attenuation)} \quad = \quad -20\log 10\,\delta_s$$
$$A_p \quad \text{(passband ripple)} \quad = \quad 20\log 10\,(1+\delta_p)$$

The difference between δ_s and δ_p is the transition width of the filter. Another important parameter is the filter length, N, which defines the number of filter.

KAISER WINDOW

The width of the main lobe and attenuation of side lobes depends only upon length 'M', i.e, length of the window. Kaiser window allows separate control of width of the main lobe and attenuation of the sidelobe. A simple approximation of the window using Bessel functions, as discovered by Jim Kaiser can be given by the formula:

$$w(n) = \frac{I_0\left(\pi\alpha\sqrt{1-\left(\frac{2n}{N-1}-1\right)^2}\right)}{I_0\,(\pi\,\alpha)} \quad ; \quad \textbf{for } \mathbf{0 \le n \le M}$$
$$\mathbf{0} \quad ; \quad \textbf{elsewhere}$$

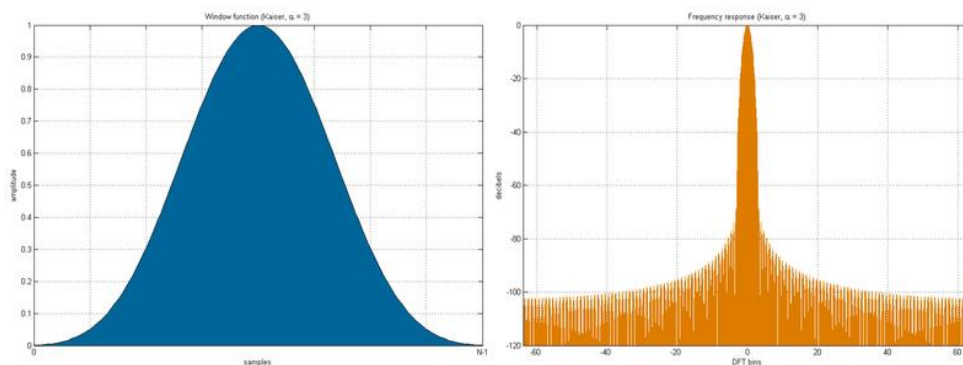**Fig. 2. Kaiser Window, α =2; B=1.5**

The lowpass, highpass, bandpass and bandreject filters have been implemented on FPGA. The filter specifications are real world and Kaiser Windowing method used to design the filter coefficients. These

coefficients are used to implement filter on Xilinx FPGA Spartan 3E kit using Xilinx ISE 10.1. Filtering is a technique to modify the frequency property of the input signal x (n) to meet certain design requirements. Broadly, it can be said as a numerical procedure, or algorithm that transfers a given sequence of No's into a second sequence that has some more desirable properties, such as less noise or distortion. A digital filter consist of the inter connection of three simple elements, adders, multipliers and delays.

Filter Specifications: The requirements for a filter are normally specified in the frequency domain in terms of the desired magnitude response and/or the desired phase (delay) response. It is desired to preserve signal components in the region called *passband* of the filter, and to reject signal components in the region called the *stopband* of the filter.

Approximation Criteria: Three different error measures have been used in designing digital filters:

1. Minimax Error Designs
2. Least-Squared Error Designs
3. Maximally Flat Approximations

FIR FILTER DESIGN USING WINDOW TECHNIQUE

Fixed Window Functions: The Gibbs phenomenon can be reduced by using a less abrupt truncation of the Fourier series. This is achieved by using a window function that tapers smoothly towards zero at both ends. There are some of the well-known fixed window functions $\omega[n]$ depending on the type of the window like *Rectangular, Bartlett, Hann, Hamming* or *Blackman*. These linear-phase filters can also be characterized by the property that only M+1 multipliers are needed in the actual implementation because of the symmetry in the filter coefficients. For these fixed window functions, the only adjustable parameter is M, half the filter order. These window functions suffer from the drawback that stopband attenuation cannot be varied. Only passband and stopband edge can be adjusted by properly selecting ωc and M.

CONCLUSIONS

The FIR filters are widely used in digital signal processing and can be implemented using programmable digital processors. But in the realization of large order filters the speed, cost, and flexibility is affected because of complex computations. So, the implementation of FIR filters on FPGAs is the need of the day because FPGAs can give enhanced speed. This is due to the fact that the hardware implementation of a lot of multipliers can be done on FPGA which are limited in case of programmable digital processors. In this thesis, a low-pass, bandpass, bandreject and

highpass FIR filter are implemented in Spartan-III-xc3s200c-4tq144 FPGA. The Direct-form structures of these filters are implemented. This approach gives a better performance than the common filter structures in terms of speed of operation, cost, and power consumption. In the Direct-form structure, N Shift Registers, N Adder and M+1 multipliers are used to realize the N order lowpass , high pass, bandpass and bandreject filter. The designed filters can work for real time processing of any digital signal. In this thesis, digital FIR filter has been designed by using Kaiser windows. The design of the filter is formulated as a problem of optimizing $I_0(x)$ and the adjustable parameter α , has been selected . So as to optimise the mainlobe width. We can achieve direct control over the stopband attenuation thereby sustaining optimality and flexibility.

In the future scope of this work, the A/D and D/A converter can be interfaced within the FPGA. The optimization of the design can be done in terms of area occupied on chip.
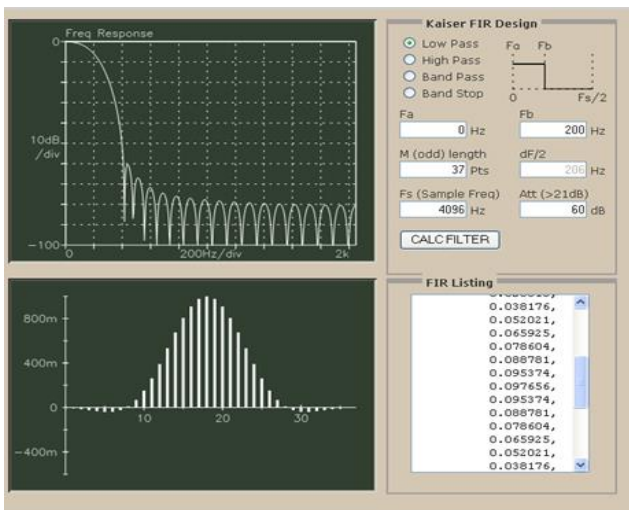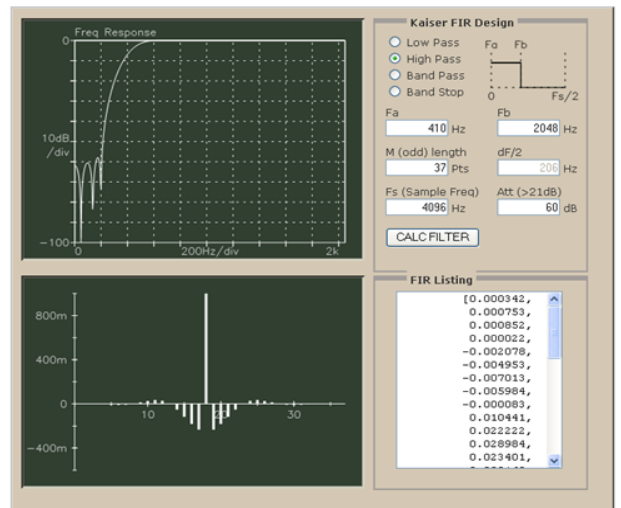

Fig. 3 Kaiser FIR Design for LPF
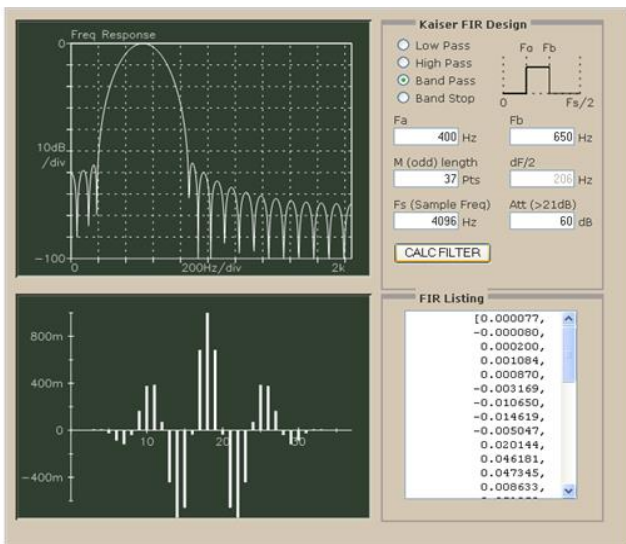

Fig. 4 Kaiser FIR Design for HPF
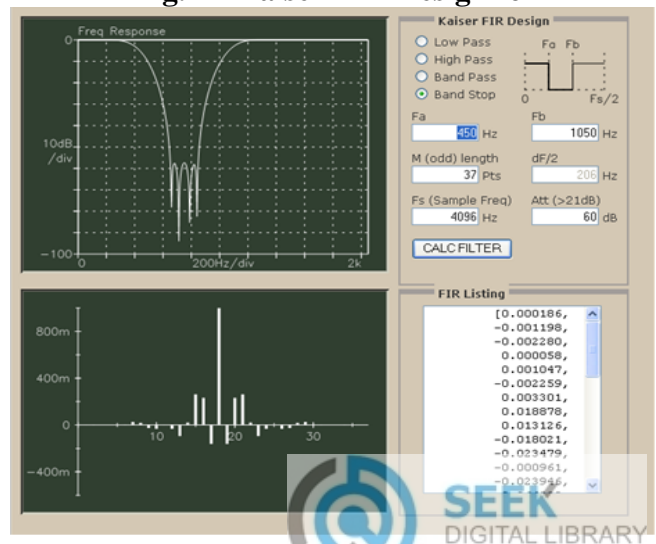

Fig. 5 Kaiser FIR Design for BPF

Fig. 6 Kaiser FIR Design for BRF

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