Proc. of the Intl. Conf. on Advances In Engineering And Technology - ICAET-2014

ISBN: 978-1-63248-028-6 doi: 10.15224/ 978-1-63248-028-6-02-25

Design and Analysis of 8T Full Adder Cell Using Double Gate MOSFET

[Ruchika,*Tripti Sharma and K. G. Sharma]

***Abstract*— This paper presents a design of a 8 transistor one-bit full adder cell with Double Gate MOSFET. This design has been compared with existing 8 transistor one-bit full adder cell using Single Gate MOSFET at 45nm technology in sub threshold region. In this paper, the designed circuits are observed keeping the power consumption and Power Delay Product as parameters. Simulations are performed on SPICE tool and they have verified the correct operation of the full adder cell using Double Gate MOSFET for a variety of inputs at different supply voltages, temperatures and frequencies. Results indicated that the full adder with Double Gate MOSFET is capable of significant improvement in power consumption and Power Delay Product.**

***Keywords*—DG MOSFET, full adder, low power, PDP, subthreshold.**

I. Introduction

The tremendous demand for the low power and high performance designs has grown significantly in recent years and this has been due to the fast growth of battery operated portable devices. Further, the aggressive scaling of transistor size for high performance applications necessitates the integration of new device structures. The Double Gate MOSFETs are example of this, which are capable for nanoscale integrated circuits. Double Gate MOSFET (DG MOSFET) is widely used in ultra-low power design. When devices are scaled, leakage and short channel effects (SCEs) such as the sub threshold slope and the drain induced barrier lowering (DIBL) became prominent. The front and back gates are electrically coupled together in Double Gate devices and this reduces the short channel effect and sub threshold leakage. The use of two gates leads to the increase in current driving of Double Gate and hence the circuit with Double Gate transistor can be operated at much lower input and threshold voltages compared to Single Gate MOSFET circuit and these means lower power consumption. The intimate coupling between the gates and the channel makes DG MOSFET technology the most scalable of all MOSFET designs [1]. Due to the presence of two gates, no part of the channel is far away from the gate. The voltage applied on the gate terminals control the electric field, determining the amount of current flow through the channel. This gives the ideal sub threshold slope for sub threshold operation [2]. Because of better control on short channel effect, Double Gate MOSFET is used for sub threshold circuit design.

Ruchika, *Tripti Sharma and K. G. Sharma
ECE Department
FET-MITS (Deemed University)
Lakshmangarh-332311, Distt.- Sikar, Rajasthan, INDIA

Sub threshold circuits operate with a supply voltage less than the threshold voltage of the MOS transistor. The use of sub threshold circuit designing in fast and energy efficient circuits is always needed in electronics industry especially in DSP, image processing and arithmetic units in microprocessors. Addition is the most basic arithmetic operation and adder is the most fundamental arithmetic component of the processor. Thus, it is worthwhile design a full adder cell with DG MOSFET and study the behavior we obtain moving towards Double Gate technology.

The paper is organized into five sections. Section I gives the general picture from where the inspiration for this research comes from. Section II illustrates the existing 8 transistor full adder cell as reported in the literature. Section III introduces the 8 transistor full adder cell using DG MOSFET. Simulations and comparison are included in Section IV and finally Section V concludes the paper.

II. 8T Full Adder with Single Gate MOSFET

A one-bit full adder circuit adds three one-bit binary numbers namely A, B, CIN. The circuit produces a two one-bit binary numbers; SUM and COUT (carry). The expressions for the sum and carry are given by equation 1 and equation 2.

$$SUM = A \oplus B \oplus CIN \quad (1)$$

$$COUT = AB + CIN\,(A \oplus B) \quad (2)$$

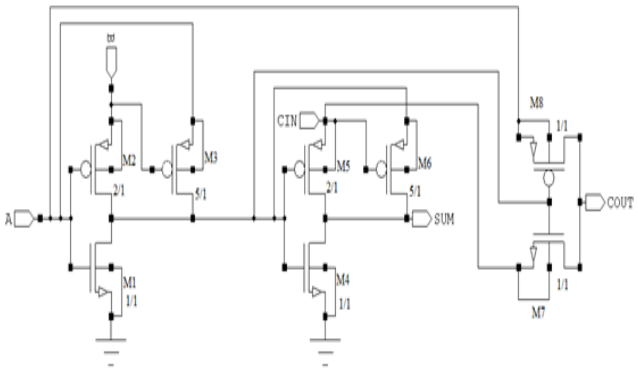

Figure 1. Schematic of 1-bit 8T Full adder with Single Gate MOSFET

The schematic of 8T transistor 1-bit full adder cell with Single gate MOSFET (SG MOSFET) is shown in Fig. 1 [3]. Two exclusive OR using 3T XOR gate [4] are cascaded to obtain the sum output of three inputs in accordance with the equation 1 and 2T multiplexer is used to implement the carry output in accordance with the equation 2. Transistors M1-M3

Proc. of the Intl. Conf. on Advances In Engineering And Technology - ICAET-2014

ISBN: 978-1-63248-028-6 doi: 10.15224/ 978-1-63248-028-6-02-25

forms the first stage of XOR gate. This XOR design is based on a modified version of a CMOS inverter using Single Gate MOSFET and a p-type Single Gate MOSFET pass transistor. When the input B is at logic high, transistor M1, M2 functions like a normal CMOS inverter during the first stage of XOR design. Thus, the output of first stage of XOR is complement of the input A. When the input B is at logic low, the CMOS inverter is at high impedance and the pass transistor M3 gets enabled and the output of the first stage of XOR design gets the same logic value as input A. Typical values of the W/L ratios for transistors M1, M2, M3 are 1/1, 2/1, 5/1. Transistors M4-M6 forms the second stage of XOR gate and works in the same manner as explained for first stage of XOR design. Typical values of the W/L ratios for transistors M4, M5, M6 are same as the corresponding ones in 3T XOR of first stage. The W/L ratios of transistors M7 and M8 are taken as 1/1.

III. Proposed 8T Full Adder using DG MOSFET

Double Gate MOSFET has been designed using the equivalent approach. DG MOSFET will be constructed by connecting two Single Gate MOSFET transistors in parallel in such a way that their source and drain are connected together [5] and [6]. DG MOSFET can be configured in two modes such as Symmetrically Driven Double Gate (SDDG) MOSFET and Independent Driven Double Gate (IDDG) MOSFET. The major difference between the two lies in the way the gates are biased. In SDDG mode, front and back gates are connected together and in IDDG mode, separate biasing are provided to the front and back gates [7].

The schematic of 8T transistor 1-bit full adder cell shown in Fig. 2 has been implemented using SDDG MOSFET. To implement new topology of 8T full adder, conventional MOSFET devices are replaced with new DG MOSFET devices. Two exclusive OR using 3T XOR gates of SDDG MOSFETs are cascaded to obtain the sum output of three inputs and to implement the carry output, 2T multiplexer design of SDDG MOSFET is used. The final sum is obtained using wired OR logic. The two gate electrodes of p-type four terminal DG MOSFET and n-type four terminal DG MOSFET are electrically connected to each other for symmetrical mode of operation. This design works efficiently in sub threshold region.

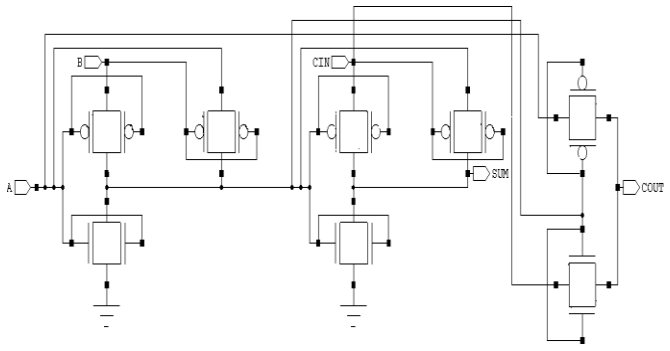

Figure 2. Schematic of 1-bit 8T Full adder using DG MOSFET

Since the mobility of holes differs from the mobility of electrons, when a CMOS circuit is implemented using Single Gate MOSFETs, the channel width (width of flow of current) of a p-type MOSFET must be about twice as large as the channel width of an n-type MOSFET in order to adjust the currents associated with the p-type and n-type MOSFET. This causes an increase in chip area. According to the DG MOSFET, however the chip area of a p-type DG MOSFET and n-type DG MOSFET are substantially the same, and the amounts of current associated with the n-type and p-type DG MOSFET can also be the same. The W/L ratios of transistors are taken as 1/1.

IV. Simulations and Comparison

In low power applications area, power consumed by the device and Power Delay Product are the main technical aspects to prefer a design over the other contending designs. The 8T full adder using Double Gate MOSFET and Single Gate MOSFET are simulated and analysed at 45nm technology. The designs are observed keeping power consumption and Power Delay Product (PDP) as parameters at different voltages, temperatures and frequencies.

A. *Variation with Voltage*

When voltages are varied then accordingly power consumption and delay changes, power consumption and PDP goes to increase as voltage increases. Other parameters like temperature and frequency are kept constant for voltage variation as temperature is taken at room temperature i.e. 25 ^{O}C and frequency at 100 MHz.

The graph shown in Fig. 3 reveals that the power consumption of 8T full adder using Double Gate MOSFET is approximately reduced by 22% as compared to 8T full adder using Single Gate MOSFET and delay introduced by the 8T full adder using DG MOSFET is also extracted for the PDP plot and found that it is also lower than the 8T full adder using Single Gate MOSFET. Due to this, there is overall remarkable reduction in power delay product of 8T full adder using Double Gate MOSFET when compared with the 8T full adder using Single Gate MOSFET as plotted in Fig. 4. This shows the superiority of DG MOSFET. Thus it can be better option for low power design.

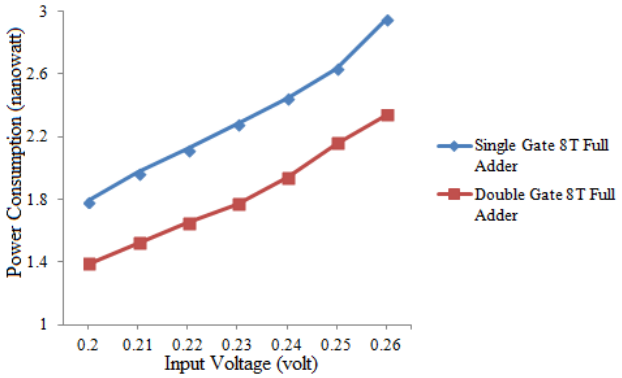

Figure 3. Power consumption versus input voltage

Proc. of the Intl. Conf. on Advances In Engineering And Technology - ICAET-2014

ISBN: 978-1-63248-028-6 doi: 10.15224/ 978-1-63248-028-6-02-25

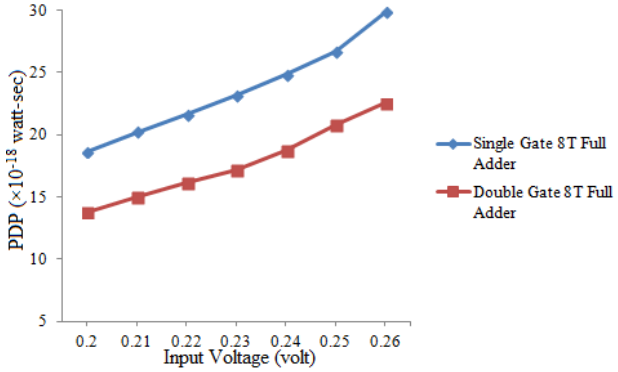

Figure 4. PDP versus input voltage

B. *Variation with Frequency*

When frequencies are varied then accordingly power consumption, delay and hence power delay product changes. The value of these frequency variations are taken at a sub threshold voltage of 0.2V and room temperature i.e. 25 ^{O}C. Power consumption increases with the increase in frequency and as power and delay have inverse relationship with each other, hence overall PDP will decrease.

The behavior of 8T full adder circuit using Double Gate MOSFET and Single Gate MOSFET are examined and plotted as illustrated in Fig. 5 and Fig. 6 for sub threshold region at various frequencies. The two designs are compared up to 300 MHz frequency. It can be seen from the graphs that the power consumption for DG MOSFET design of 8T full adder is lower for higher frequencies and PDP is very much reduced for the 8T full adder circuit using DG MOSFET. This ensures the better performance of Double Gate MOSFET circuit for high frequency applications over Single Gate MOSFET circuit.

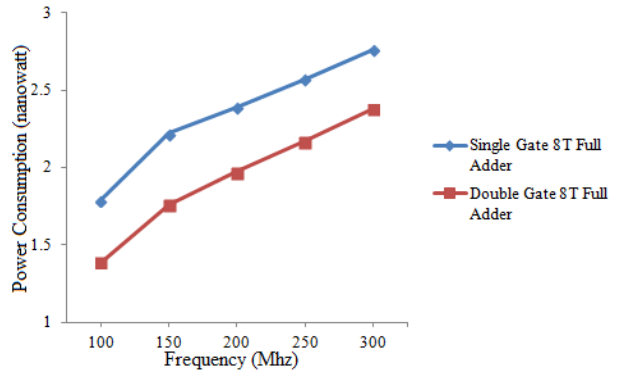

Figure 5. Power consumption versus frequency

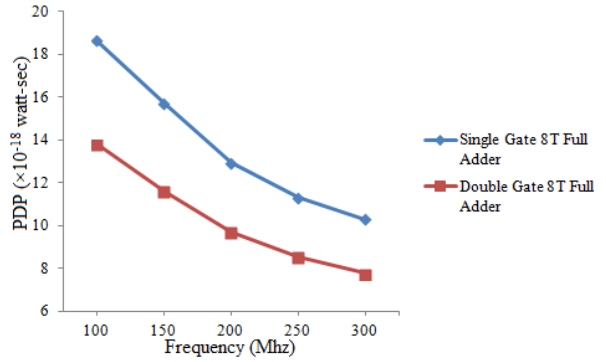

Figure 6. PDP versus frequency

C. *Variation with Temperature*

The value of temperature variations are taken in sub threshold region with input voltage of 0.2V and frequency 100 MHz. Power consumption of the device increases with temperature as the collision rate of the carriers increase and some of the power is consumed in the form of thermal energy. With increase in temperature, there is a decrease of about 15% to 20% in power consumption of 8T full adder circuit with DG MOSFET and significant decrement in delay results into reduced power delay product for DG MOSFET design of 8T full adder circuit as depicted from Fig. 7 and Fig. 8.

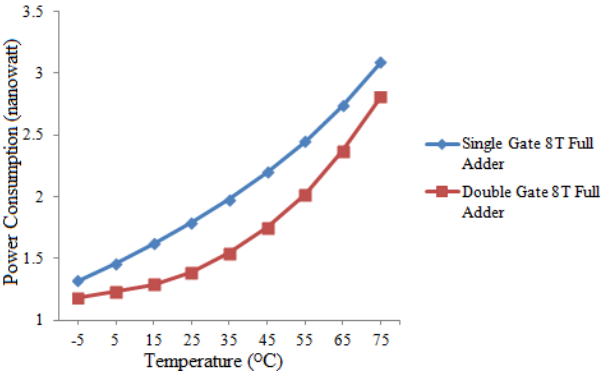

Figure 7. Power consumption versus temperature

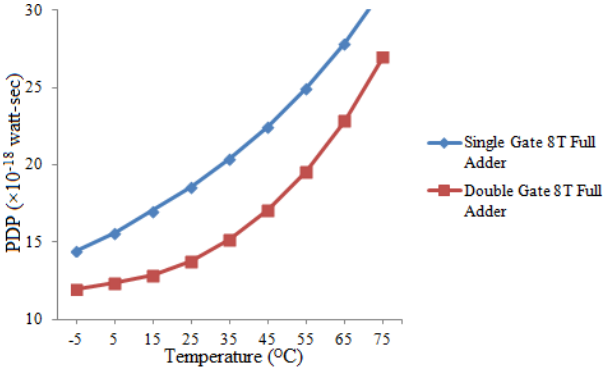

Figure 8. PDP versus temperature

From the mentioned comparisons, it is clear that the one of the main constraint in low power VLSI design i.e. power delay

Proc. of the Intl. Conf. on Advances In Engineering And Technology - ICAET-2014

ISBN: 978-1-63248-028-6 doi: 10.15224/ 978-1-63248-028-6-02-25

product of the DG MOSFET design is always reduced to remarkable extend irrespective of incorporated parameters such as voltage, frequency and temperature.

v. Conclusion

The one-bit 8T full adder using DG MOSFET has been designed and compared with one-bit 8T full adder with Single Gate MOSFET. Comparisons are done at various parameters such as input voltage, frequency and temperature. The remarkable reduction in power consumption and as well as in the Power Delay Product has been observed in the DG MOSFET design of 8T full adder during the simulation makes it better than the SG MOSFET design of 8T full adder. It is found that the DG MOSFET full adder circuit operates at higher speed than the SG MOSFET full adder circuit while maintaining the desired digital characteristics. The analysis of the simulated results confirms the feasibility of DG MOSFET technique in digital design. Hence DG MOSFET technology is more suitable for low power circuit performance.

References

[1] George James T, S. Joseph and V. Mathew, "Effect of Counter-doping Thickness on Double-Gate MOSFET Characteristics," Journal of Semiconductor Technology and Science, Vol. 10(2), pp. 130-133, June 2010.

[2] S. K. Gupta, G. G. Pathak, D. Das and C. Sarma, "Design and Simulation of a Two Stage OPAMP Using DG MOSFETs for Low Power and Low Voltage Applications," International Journal of Wisdom Based Computing, Vol. 1(3), pp. 60-63, December 2011.

[3] Shiwani Singh, T. Sharma, K. G. Sharma and Prof. B.P.Singh, "PMOS based 1-bit Full Adder Cell," International Journal of Computer Applications, Vol. 42(15), pp. 6-9, March 2012.

[4] S. R. Chowdhury, A. Banerjee, A. Roy, H. Saha, "A high speed 8-transistor full adder design using novel 3 transistor XOR gates," International Journal of Electronics and Systems, Vol. 2(4), pp. 217-223, 2008.

[5] A. K. Shrivastava and S. Akashe, "Comparative Analysis of Low Power 10T and 14T Full Adder using Double Gate MOSFET," International Journal of Computer Applications, Vol. 75(3), pp. 48-52, August 2013.

[6] M. Reyboz, O. Rozeau, T. Poiroux, P. Martin, "Asymmetrical Double Gate (ADG) MOSFETs Compact Modeling," LETI–CEA, France, 2005.

[7] R. Kushwah and S. Akashe, "Design and Analysis of Tunable Analog Circuit using Double Gate MOSFET at 45nm CMOS Technology," 3rd IEEE International Advance Computing Conference (IACC), pp. 1589-1594, 2013.

About Author (s):

RUCHIKA received her B.E. degree in Electronics and Communication Engineering from Apeejay College of Engineering, Gurgaon. She is pursuing her M.Tech degree in VLSI Design from Faculty of Engineering & Technology of Mody Institute of Technology & Science, Lakshmangarh, Rajasthan. Her research interests are low power, high performance digital design.

DR. TRIPTI SHARMA earned B.E. degree in Electronics Engineering from North Maharashtra University in 2001 and M. Tech. degree in VLSI Design from Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan in 2010 as well as achieved Ph.D. in the field of low power high performance digital VLSI circuit design from Suresh Gyan Vihar University, Jaipur. After stepping into professional world, she started as lecturer with C.S.J.M University, Kanpur and continued it up to late 2003. After that she joined Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan. Her working habits and discipline made her popular among the university and she was later awarded with designation of Asst. Professor in 2009. Her current research interests include low power digital VLSI circuits. She has more than 45 papers published in International Journals and International / National Conferences. Dr. Sharma is the life member of Indian Society of Technical Education (ISTE).

DR. K. G. SHARMA received the B.E. degree in Electronics and Communication Engineering from Madan Mohan Malviya Engineering College, DDU University, Gorakhpur in 2001 and completed his M Tech. degree in VLSI Design from Faculty of Engineering & Technology, Mody Institute of Technology and Science in 2009. He acheived his Ph.D. degree in the field of low power VLSI circuits from from Suresh Gyan Vihar University, Jaipur. He demonstrated his skills in Research & Development of Industrial Electronics, Kanpur for a briefer period and then he shifted to Academics and shared his knowledge as lecturer at renowned university in Kanpur in the initial stages of his career. He extended his profession as faculty of Engineering and Technology in MITS from 2003 and with experience promoted to Asst. Professor in the same university. Because of his extensive research work, he has more than 46 research papers published in various international/ national journals and conferences. Dr. Sharma is the life member of Indian Society of Technical Education (ISTE).