

Radiation tolerance experiment for a dynamically reconfigurable vision architecture

Minoru Watanabe and Shoji Kawahito

Abstract— Recently, autonomous vehicles and robots demand high-speed image recognition capability that is superior to that of the human eye, in addition to capability of recognizing various natural images just like humans can. However, to realize both, the bus bandwidth of current memories is insufficient. Such an embedded system necessitates the use of numerous high-resolution template images on a memory. Although the amount of memory is always sufficient, the transfer speed of template images is insufficient. To increase the number of recognition images, the number of template images must be increased. In addition to realizing rapid recognition, numerous template images must be transferred to a processor. Then a matching operation must be executed within an extremely short period. However, achieving such high-speed real-time image recognition operation is difficult because of the bottleneck of the bus bandwidth between the memory and processor. A dynamically reconfigurable vision architecture is suitable to alleviate that bottleneck. This paper presents radiation tolerance analysis of configuration contexts on a holographic memory used for the dynamically reconfigurable vision architecture.

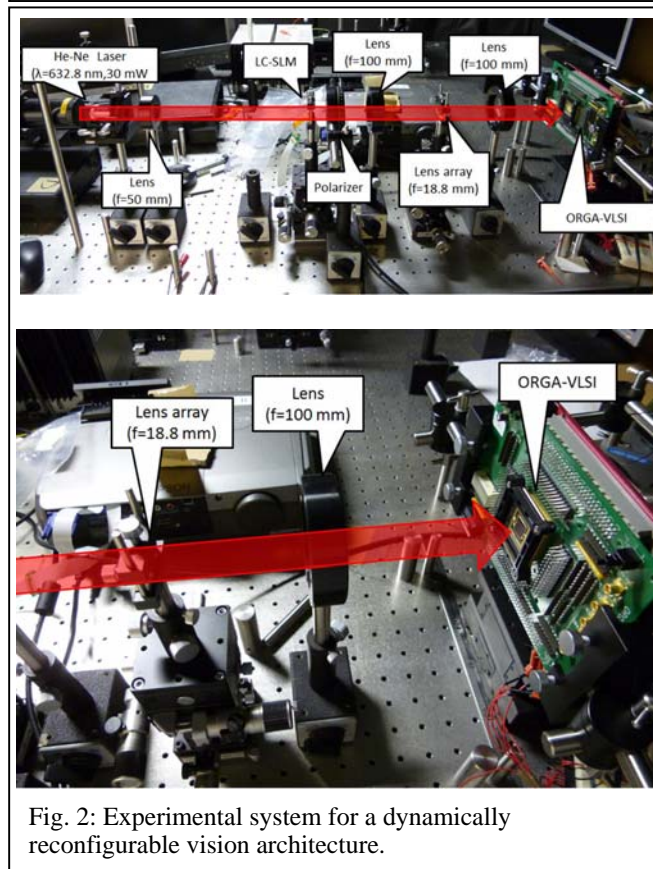
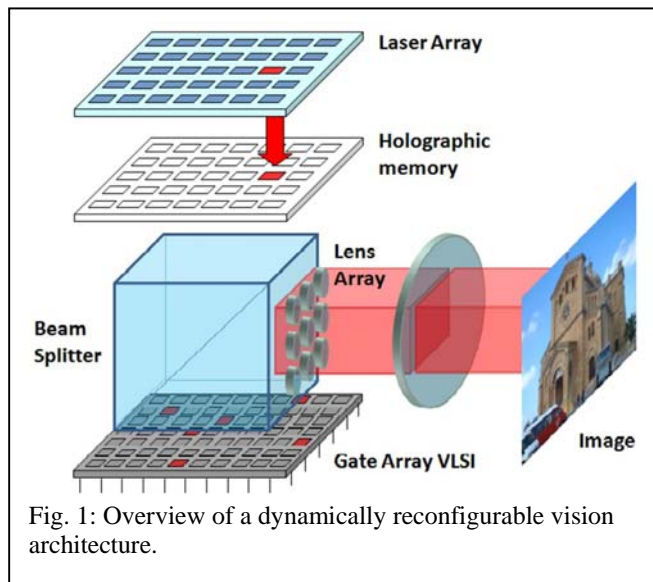
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I. Introduction

Recently, autonomous vehicles and robots have come to require high-speed image recognition capability that is superior to that of the human eye, as well as recognition capability of various natural images just like that of a human being [1][2]. Frame rates for the image recognition of almost all such systems are limited to 30 frames per second (fps) [3][4]. However, such embedded systems must execute visual processing operations at rates higher than 1,000 fps to realize a safer system with performance surpassing that of the human eye and brain [5][6]. Recently, space systems demand such high-speed image recognition [7]. Therefore, highly radiation-tolerant, high-speed image recognition systems are needed.

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Conventional image recognition systems have been impaired by bottlenecks that impede the transfer of data between an image sensor or a CCD camera and a processing unit. Therefore, various analog vision chips and digital vision chips have been developed to include both an image sensor and a type of processing element [8][9][10]. Now, gigahertz-order transfer speed can be achieved. Therefore, the bottleneck for the transfer between an image sensor or a CCD camera and a processing unit has been removed. Modern image recognition systems invariably consist of an image sensor and an embedded processor system connected to the image sensor.

Nevertheless, recent image recognition systems still have a bottleneck between the processor and memory. To recognize many images, many template images must be stored in memory and must be sent to the processor. Inside the processor, comparison operations between the external image and template images are executed. Along with the increase in the number of recognition patterns, many template images must be transferred to the processor. Nevertheless, that image recognition operation must be completed within 1 ms to realize a high-performance visual device that is superior to the human eye. In this case, the memory transfer speed has become a new bottleneck.

For example, assuming that a template image has $1,024 \times 1,024$ pixels with each pixel having a single bit of information, then 100,000 image patterns must be recognized in less than 1 ms. Consequently, the transfer rate becomes as high as 13.1 TB/s. Such a rate is extremely difficult to achieve under current VLSI technologies.

Recently, optically reconfigurable gate arrays (ORGAs), which consist of a holographic memory and an optically programmable gate array VLSI, have been developed [11][12][13]. Configuration contexts stored in a holographic memory are read out optically. They can be programmed optically onto the gate array VLSI using photodiodes. Such parallel configuration can be executed at every 10 ns. Such high-speed reconfiguration capability is also useful for high-speed template image transfer. Therefore, ORGA technology is suitable for use as a high-speed image recognition system. Dynamically reconfigurable vision architectures based on ORGA architecture have been demonstrated [14][15].

Currently, satellites and rockets designed for space operations require high-speed image recognition. Dynamically reconfigurable vision systems are suitable for such space systems in terms of recognition speed and the number of recognition image patterns. However, under a space environment, radiation is frequently incident to any device inside an embedded system. Such space embedded systems face frequent temporary-errors just like soft-errors and a system down trouble understood as total ionizing dose effect. Therefore, the radiation tolerance of dynamically reconfigurable vision architecture must be clarified when the dynamically reconfigurable vision architecture must be used in a space environment.

This report therefore presents a more advanced dynamically reconfigurable vision architecture and the radiation tolerance analysis results of configuration contexts

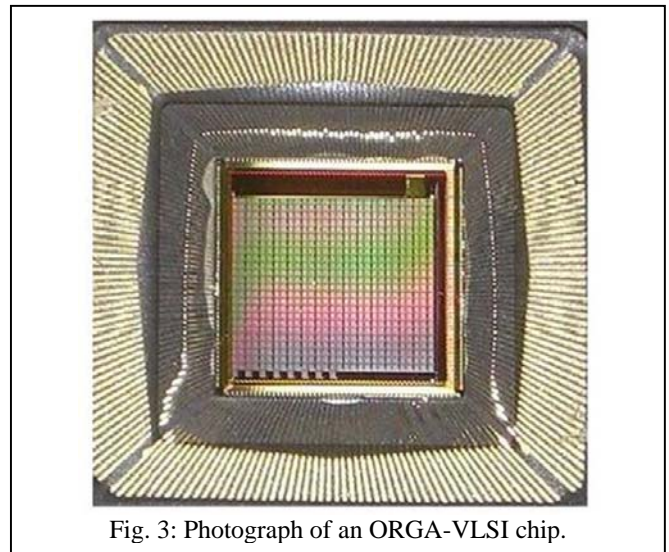


Fig. 3: Photograph of an ORGA-VLSI chip.

on a holographic memory for the dynamically reconfigurable vision architecture.

II. Dynamically reconfigurable vision architecture

Fig. 1 presents an overview of a dynamically reconfigurable vision architecture [14][15]. The dynamically reconfigurable vision architecture can recognize sample images of 100,000 kinds at every 1 ms by exploiting the storage capacity and the large bandwidth connection between a holographic memory and a programmable gate array.

The dynamically reconfigurable vision architecture comprises a laser array, a holographic memory, a beam splitter, a lens array, an imaging lens, and an optically reconfigurable gate array (ORGA-VLSI) with a fine-grained programmable gate array [12][13]. The ORGA-VLSI's function is the same as that of currently available field programmable gate arrays (FPGAs). However, ORGAs support a parallel configuration, so the ORGA reconfiguration time reaches 10 ns although FPGA's reconfiguration time is larger than 100 ms. Therefore, numerous template images are stored on a holographic memory as circuits to recognize template images. In order to recognize an external image, firstly, a circuit corresponding to a template image is programmed onto a fine-grained programmable gate array on an ORGA-VLSI. Then, next circuit is programmed onto a programmable gate array, and so on. Therefore, in order to recognize an external image, a lot of circuits corresponding to template images are dynamically programmed onto a programmable gate array within a control period of a real-time space system.

On the other hand, each time a configuration is completed, an image recognition operation is executed on a fine-grained programmable gate array. In this architecture, each template datum can be transferred to the dynamically reconfigurable vision chip in 10 ns because an ORGA architecture facilitates nanosecond-order configuration. Therefore, only 1 ms elapsed for the transfer of 100,000 templates and for their matching

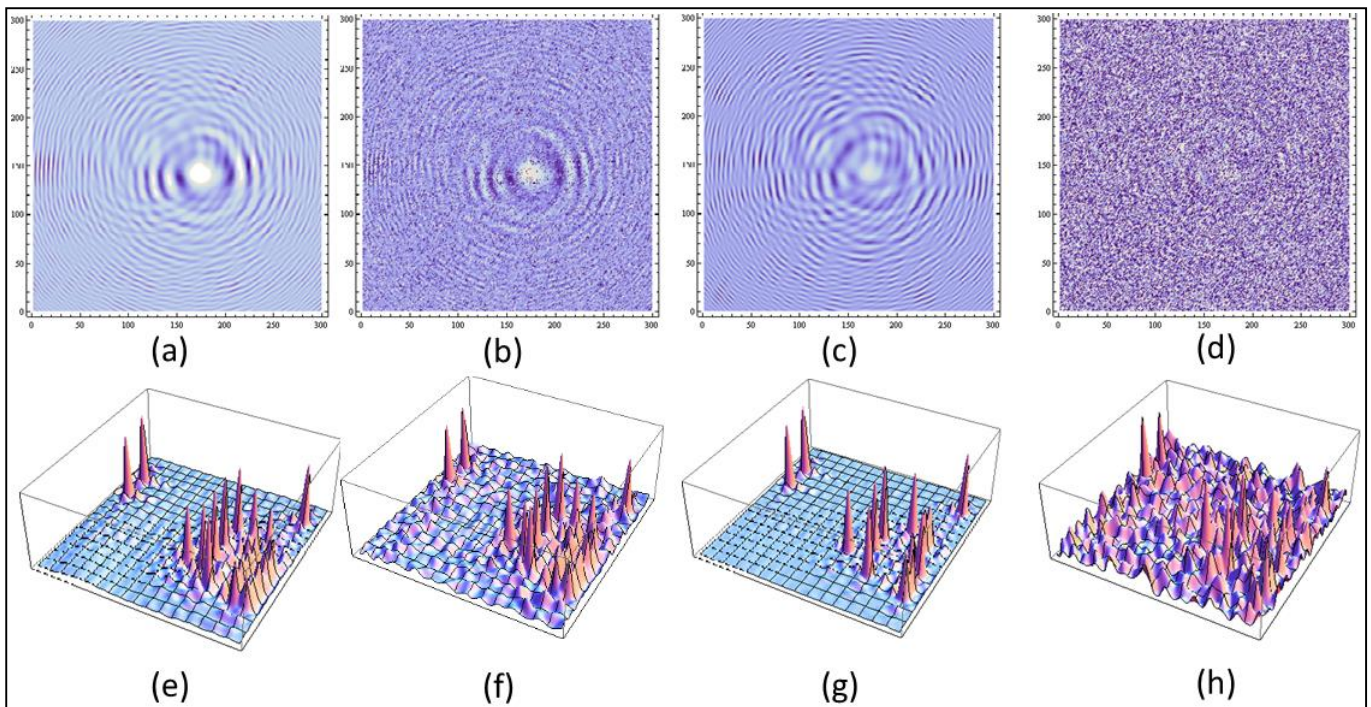


Fig. 4: Radiation simulation results. Panels (a) and (c) respectively show 300×300 pixel holographic memory patterns of an OR circuit and a majority voting circuit. Configuration context patterns generated from these holographic memory patterns are shown respectively in panels (e) and (g). High-contrast configuration context patterns can be generated. Panels (b) and (d) portray corrupt holographic memory patterns for which 17,500 and 59,000 impulse noises were applied onto original holographic memory patterns of panels (a) and (c). Even if 19.4–65.5% area on such holographic memory patterns are damaged, a correct configuration context pattern can be generated.

operations. Consequently, this architecture can enable real-time pattern matching operations inside a chip, as presented in Fig. 3.

Part of a dynamically reconfigurable vision-chip system was constructed. The experimental system is presented in Fig. 2. In this demonstration system, an image was provided from a liquid crystal spatial light modulator (LC-SLM) as an emulation. The LC-SLM used for this experiment is a projection TV panel (Seiko Epson Corp.) with $1,024 \times 768$ pixels, each of which is $12 \times 12 \mu\text{m}^2$. The light source for the image input is a 632.8 nm, 30 mW He-Ne laser. An image on the LC-SLM is transferred to an ORGA-VLSI chip through a lens array. Each pixel of the image is focused onto a photodiode of the ORGA-VLSI using a lens of the lens array. Here, an 11,424 gate count ORGA-VLSI chip was used. Fig. 3 portrays a VLSI chip fabricated using a $0.35 \mu\text{m}$ standard complementary metal oxide semiconductor (CMOS) process technology. Voltages of the core and I/O cells were designed to be identical: 3.3 V. Photodiodes were constructed between an N+ diffusion layer and a P-substrate. The size was designed as $9.5 \mu\text{m} \times 8.8 \mu\text{m}$. The photodiode cells are arranged at $34.5 \mu\text{m}$ horizontal intervals and at $33.0 \mu\text{m}$ vertical intervals. This design incorporates 37,856 photodiodes. The average aperture ratio of the overall VLSI is 4.24%. The gate array of the ORGA-VLSI uses an island style. The functionality of a gate array is fundamentally identical to that of currently available

FPGAs. In all, the gate array includes 336 logic blocks, 360 switching matrices, and 8 I/O blocks, which include 4 programmable I/O bits. In this photograph's experiment, images were detected experimentally. After the operation, circuits used to recognize the image patterns were emulated in turn on an FPGA. In this case, four images with 128×128 pixels were used. Four template matching circuits were reconfigured onto a programmable gate array so that the template-matching operations of four images were executed correctly.

III. Holographic memory radiation tolerance

In order to confirm the radiation tolerance of a holographic memory on the dynamically reconfigurable vision architecture, radiation simulation of a holographic memory for configuration data was done. Here, configuration contexts are used for image recognition operations. These real experiments already confirmed them, but practical experiments show that the results invariably depend on the position accuracy between an ORGA-VLSI and a holographic memory. The error factor was not small. Therefore, as described herein, ideal conditions with no positioning error were simulated to present the maximum performance. Figs. 4(a) and 4(b) respectively show

300 × 300 pixel holographic memory patterns of an OR circuit and a majority voting circuit. In a dynamically reconfigurable vision architecture, many templates used for template matching operations are stored in a holographic memory. Herein, we only discuss one holographic memory page. Configuration context patterns generated from these holographic memory patterns are portrayed respectively in Figs. 4(e) and 4(g). High-contrast configuration context patterns were confirmed. Panels (b) and (d) respectively show corrupt holographic memory patterns for which 17,500 and 59,000 impulse noises were applied onto original holographic memory patterns of panels (a) and (b). Even if 19.4–65.5% area on such holographic memory patterns were damaged, correct configuration context patterns could be generated. In an FPGA, if many bits on a configuration context are damaged, the FPGA cannot function correctly. However, in the dynamically reconfigurable vision architecture, even if 65.5% of the configuration data were damaged by radiation, correct configuration information could be read out from the corrupt holographic configuration data. Therefore, this architecture is robust against radiation.

IV. Conclusion

We presented a demonstration that a dynamically reconfigurable vision architecture is also useful for space systems because its architecture is highly radiation tolerant for space radiation. Even if 65.5% configuration data of the holographic memory region were damaged, the correct configuration context could be read out from the damaged holographic memory. Results demonstrate that, compared with such FPGA radiation tolerance, the dynamically reconfigurable vision architecture is extremely robust.

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References

- [1] A. Mammeri, E. Khiari, A. Boukerche, "Road-Sign Text Recognition Architecture for Intelligent Transportation Systems," IEEE Vehicular Technology Conference, pp. 1-5, 2014.
- [2] P. Y. Kang, Y. P. Chen, M. J. Jeng, "Lane recognition system implemented by a full hardware design," International Symposium on Next-Generation Electronics, pp. 1-3, 2014.
- [3] R. Johansson et al., "A 1/13-inch 30fps VGA SoC CMOS image sensor with shared reset and transfer-gate pixel control," IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 414 - 415, 2011.
- [4] N. Massari, M. De Nicola, M. Gottardi, "A 30uW 100dB contrast vision sensor with sync-async readout and data compression," ESSCIRC, pp. 138 - 141, 2010.
- [5] G. L. Cembrano, A. R. Vazquez, R. D. Castro, S. E. Meana, "A 1000FPS@128/spl times/128 vision processor with 8-bit digitized I/O," European Solid-State Circuits Conference, pp. 61 - 64, 2003.
- [6] E. Ito, S. Saga, T. Okatani, K. Deguchi, "GPU-based high-speed and high-precision visual tracking," SICE Annual Conference, pp. 2151 - 2154, 2010.
- [7] C. C. Liebe, "Pattern recognition of star constellations for spacecraft applications," IEEE Aerospace and Electronic Systems Magazine, Vol. 8, Issue 1, pp. 31 - 39, 1993.
- [8] A. Mhani, G. Sicard, G. Bouvier, "Analog vision chip for sensing edges, contrasts and motion," IEEE International Symposium on Circuits and Systems, pp. 4257 - 4260, 2010.
- [9] J.L. Wyatt, D. L. Standley, W. Yang, "The MIT Vision Chip Project: analog VLSI systems for fast image acquisition and early vision processing," IEEE International Conference on Robotics and Automation, pp. 1330 - 1335, 1991.
- [10] A. Lopich, P. Dudek, "An 80x80 general-purpose digital vision chip in 0.18um CMOS technology," IEEE International Symposium on Circuits and Systems, pp. , 2010.
- [11] T. Mabuchi, M. Watanabe, "A superimposing acceleration and optimization method of optical reconfiguration speed without any increase of laser power," Applied Optics, Vol. 49, No. 22, pp. 4120-4126, 2010.
- [12] M. Nakajima, M. Watanabe, "Optical buffering technique under space radiation environment," Optics Letters, Vol. 34, Issue 23, pp. 3719-3721, 2009.
- [13] M. Nakajima, M. Watanabe, "A four-context optically differential reconfigurable gate array," IEEE/OSA Journal of Lightwave Technology, Vol. 27, No 20, pp. 4460-4470, 2009.
- [14] H. Nakada, M. Watanabe, S. Kawahito, "Parallel Template Matching Operations on a Dynamically Reconfigurable Vision-Chip Architecture," IEEE Northeast Workshop on Circuits and Systems, pp. 205-208, 2011.
- [15] M. Yasuda, M. Watanabe, "Dynamically reconfigurable vision chip architecture," International conference on Field-Programmable Logic and its Applications, pp. 508 - 512, 2010.